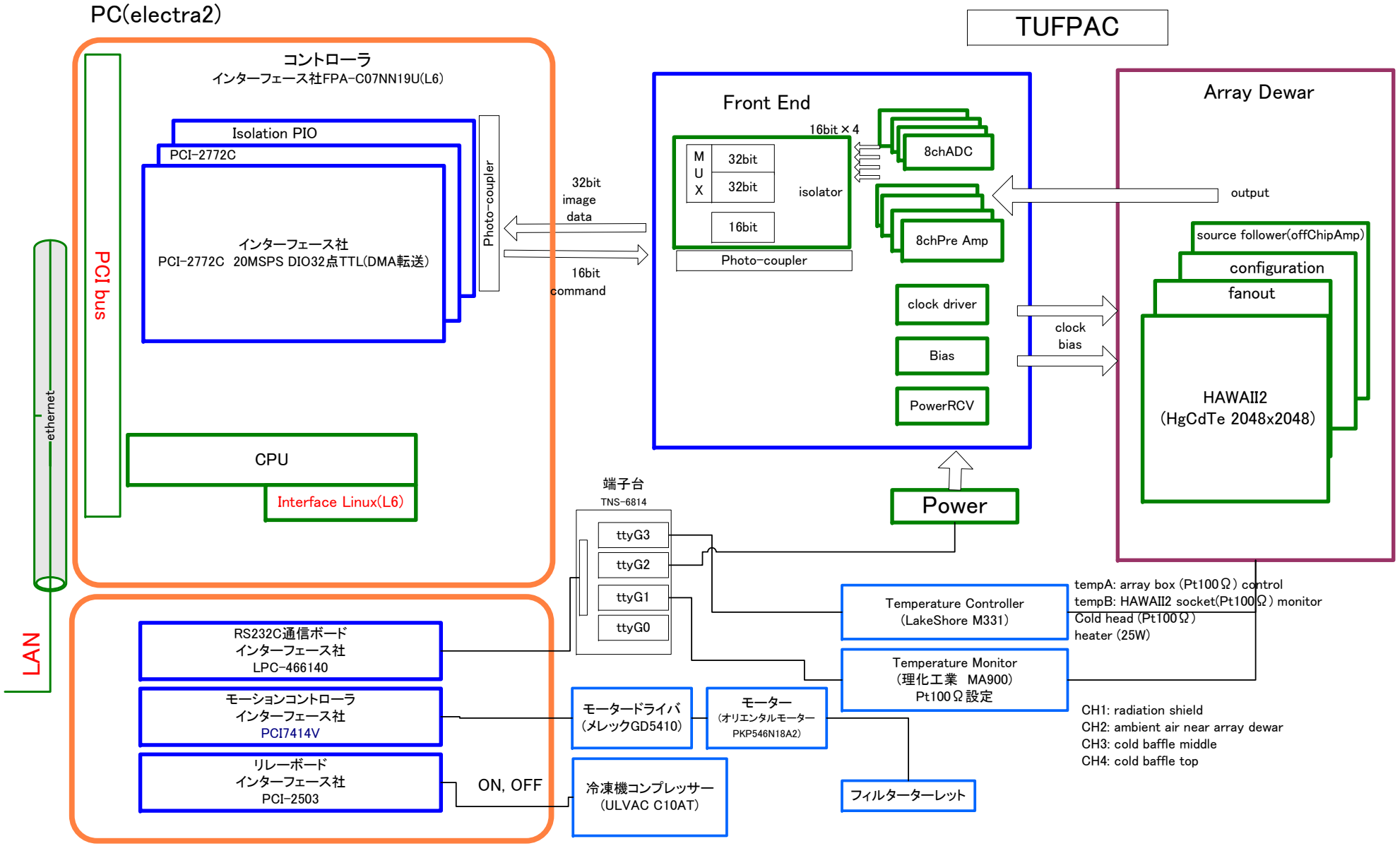
Tohoku University Array Control System (TACS)

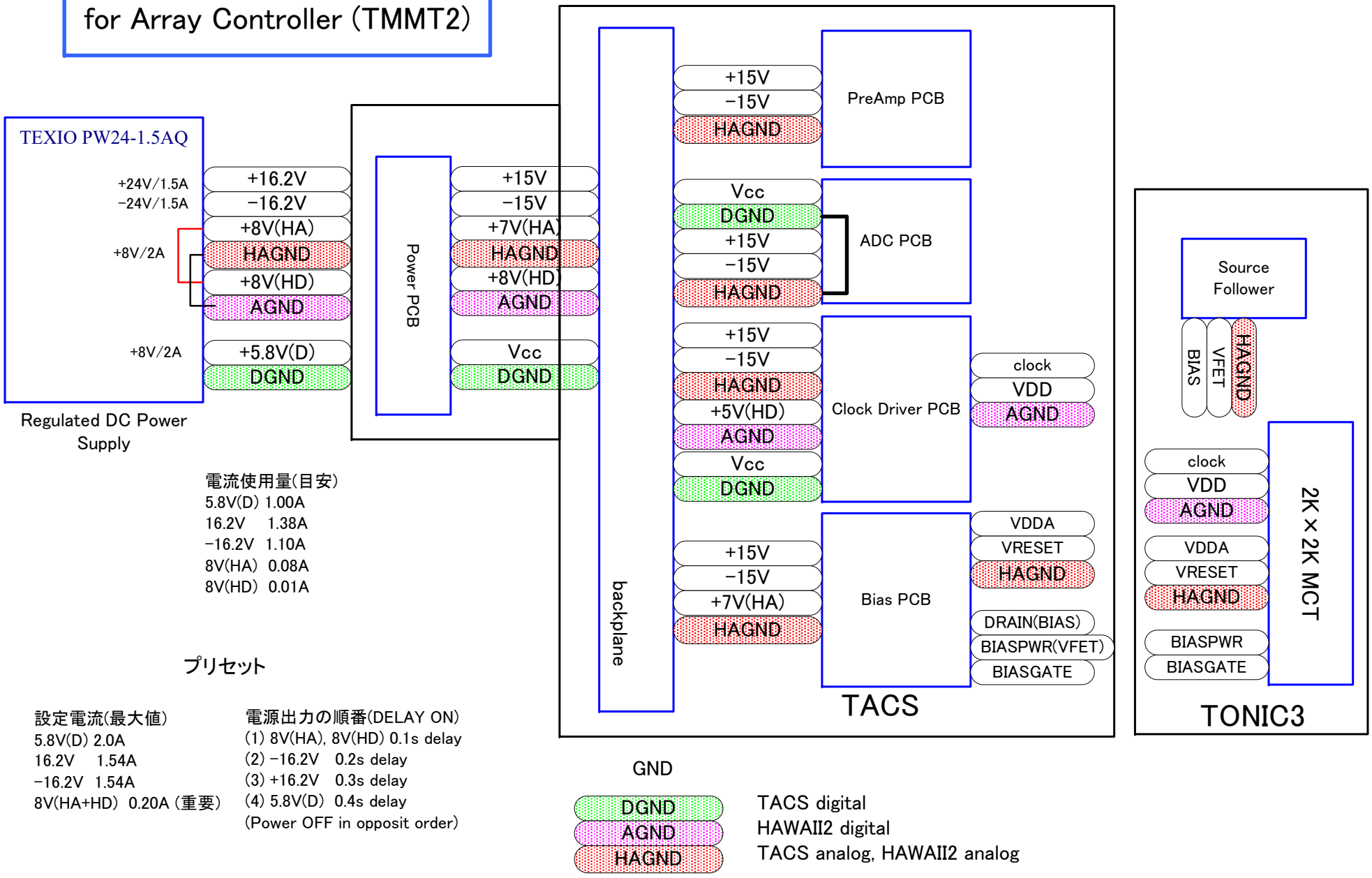
外付けアンプによるHAWAI2の32ch　no-crosstalk 読み出しシステム

2023/10/10 T. Ichikawa



Power Supply & GND for Array Controller (TMMT2)

2022/11/06 T. Ichikawa



電流使用量(目安)
5.8V(D) 1.00A
16.2V 1.38A
−16.2V 1.10A
8V(HA) 0.08A
8V(HD) 0.01A

プリセット

設定電流(最大値)
5.8V(D) 2.0A
16.2V 1.54A
−16.2V 1.54A
8V(HA+HD) 0.20A (重要)

電源出力の順番(DELAY ON)
(1) 8V(HA), 8V(HD) 0.1s delay
(2) −16.2V 0.2s delay
(3) +16.2V 0.3s delay
(4) 5.8V(D) 0.4s delay
(Power OFF in opposit order)

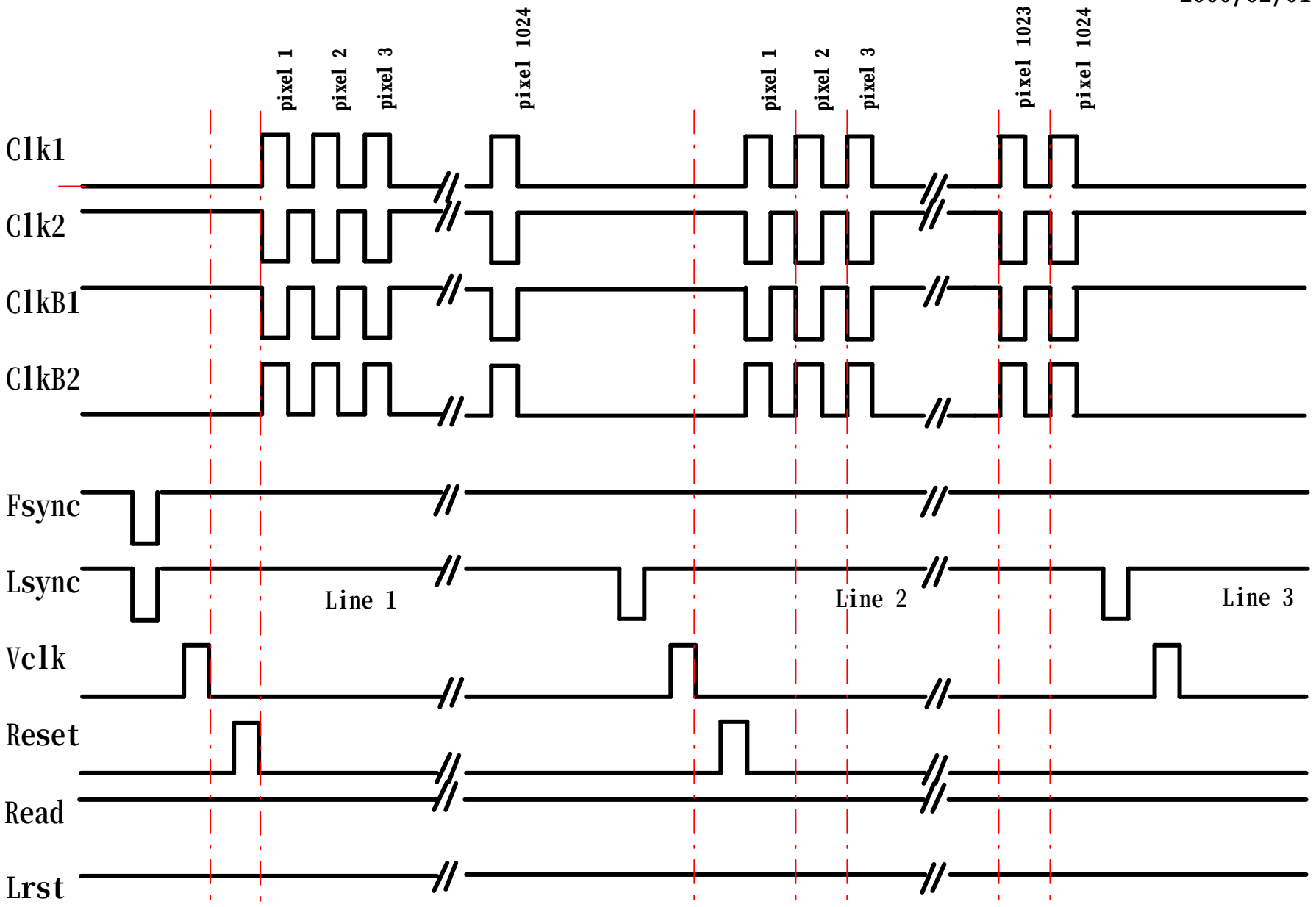
GND

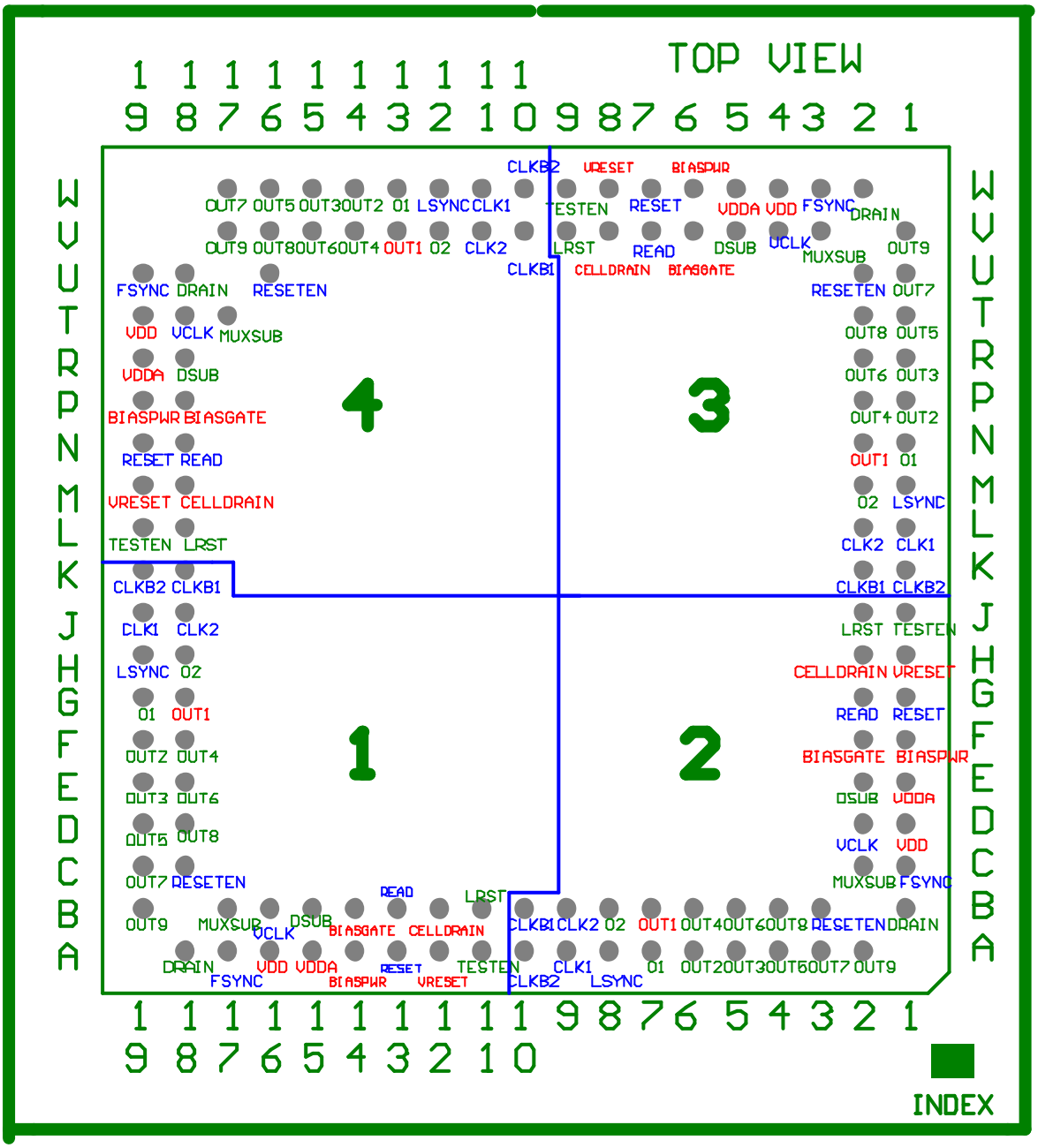
DGND
AGND
HAGND

TACS digital
HAWAII2 digital
TACS analog, HAWAII2 analog

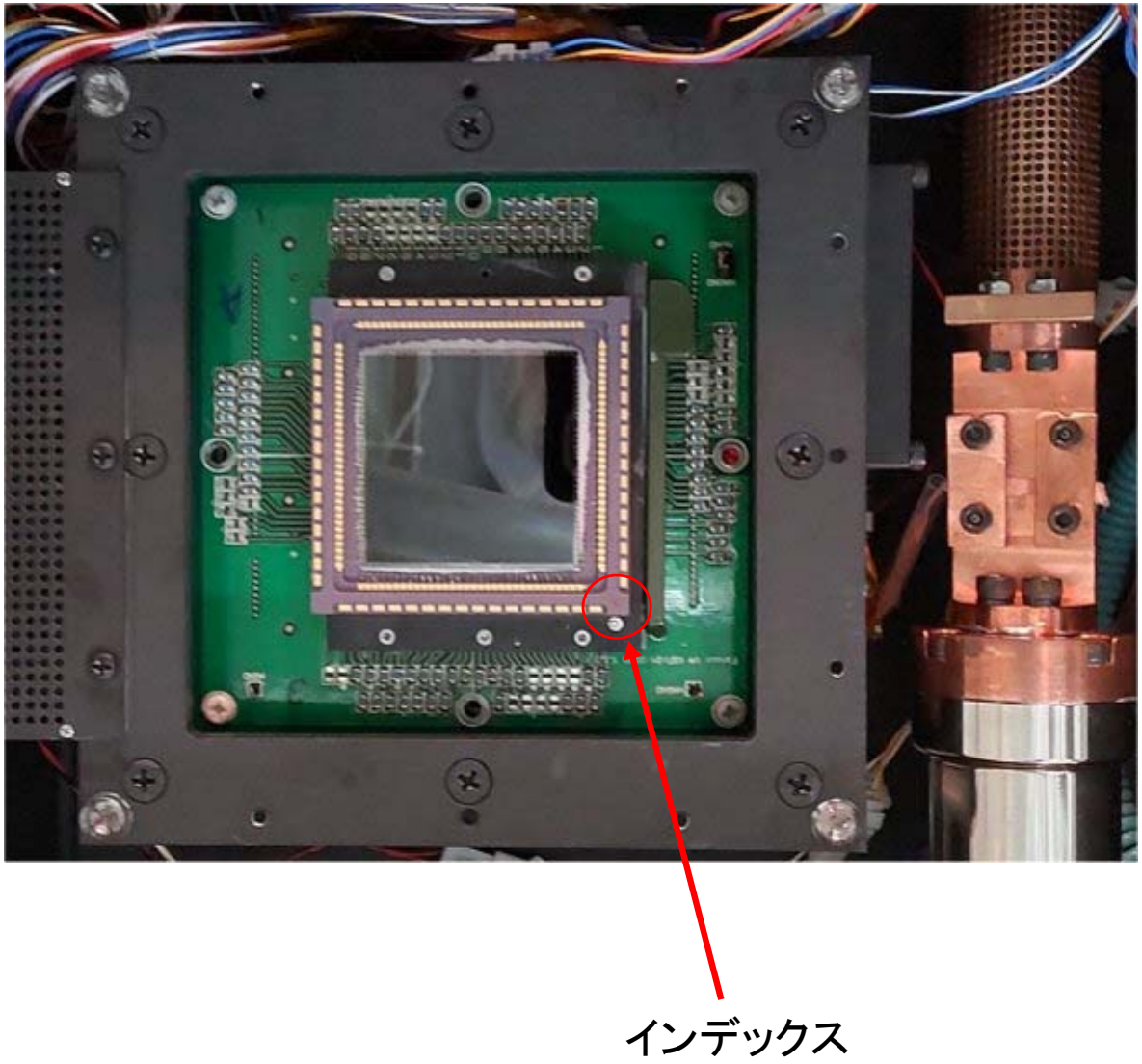
2048×2048 HAWAII2 Basic Timing for Single Output Mode

2000/02/01 市川



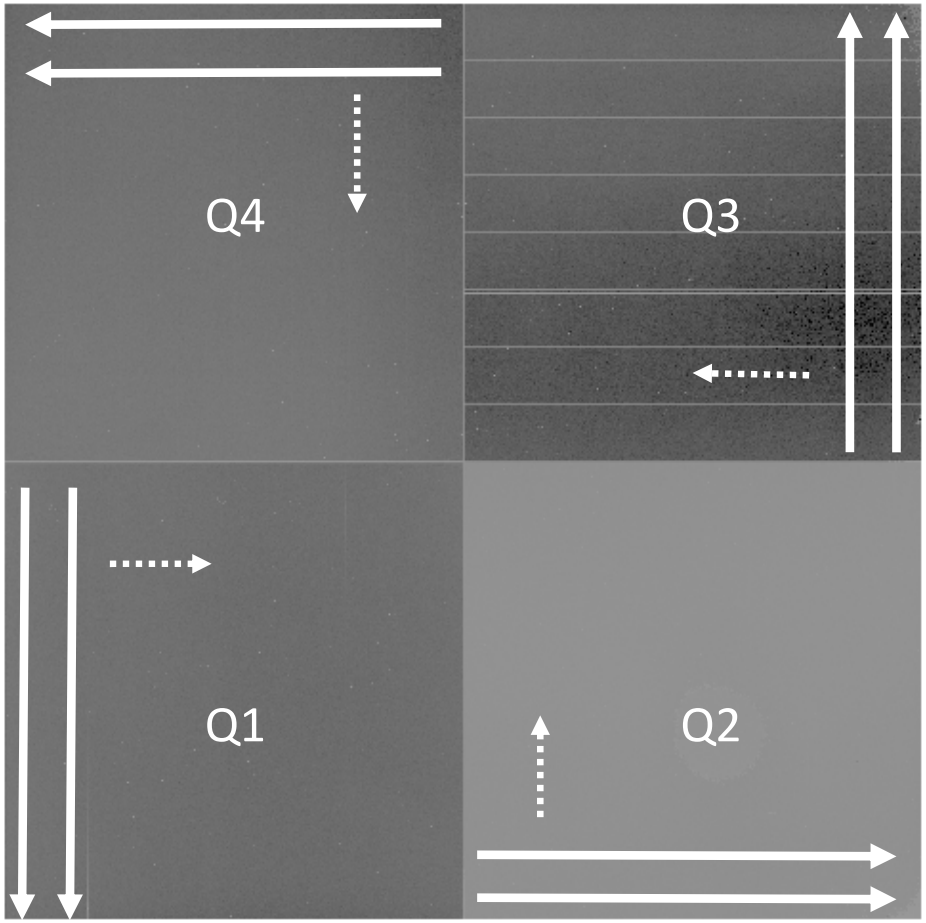

TOP VIEW
1 1 1 1 1 1 1 1 1 1
9 8 7 6 5 4 3 2 1 0 9 8 7 6 5 4 3 2 1
W V U T R P N M L K J H G F E D C B A
CLKB2 VRESET BIASPWR
OUT7 OUT5 OUT3 OUT2 O1 LSYNC CLK1 TESTEN RESET VDDA VDD FSYNC DRAIN
OUT9 OUT8 OUT6 OUT4 OUT1 O2 CLK2 LRST READ DSUB VCLK MUXSUB OUT9
CLKB1 CELLDRAIN BIASGATE
FSYNC DRAIN RESETEN
VDD VCLK MUXSUB
VDDA DSUB
BIASPWR BIASGATE
RESET READ
VRESET CELLDRAIN
TESTEN LRST
CLKB2 CLKB1
CLK1 CLK2
LSYNC O2
O1 OUT1
OUT2 OUT4
OUT3 OUT6
OUT5 OUT8
OUT7 RESETEN
OUT9
4
3
1
2
RESETEN OUT7
OUT8 OUT5
OUT6 OUT3
OUT4 OUT2
OUT1 O1
O2 LSYNC
CLK2 CLK1
CLKB1 CLKB2
LRST TESTEN
CELLDRAIN VRESET
READ RESET
BIASGATE BIASPWR
DSUB VDDA
VCLK VDD
MUXSUB FSYNC
MUXSUB VCLK DSUB BIASGATE CELLDRAIN READ LRST
DRAIN FSYNC VDD VDDA BIASPWR RESET VRESET TESTEN
CLKB1 CLK2 O2 OUT1 OUT4 OUT6 OUT8 RESETEN DRAIN
CLKB2 LSYNC CLK1 O1 OUT2 OUT3 OUT6 OUT7 OUT9
1 1 1 1 1 1 1 1 1 1 9 8 7 6 5 4 3 2 1
9 8 7 6 5 4 3 2 1 0
INDEX

HAWAII2

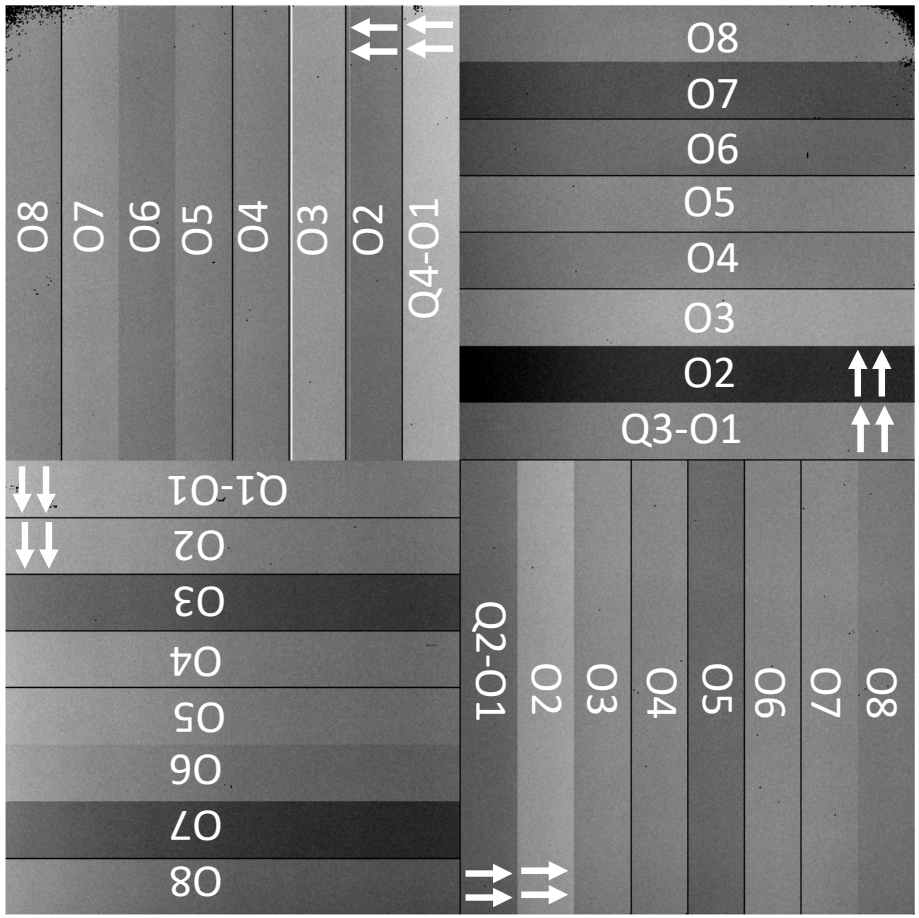


Q quad
O octant

4チャネル読み出し

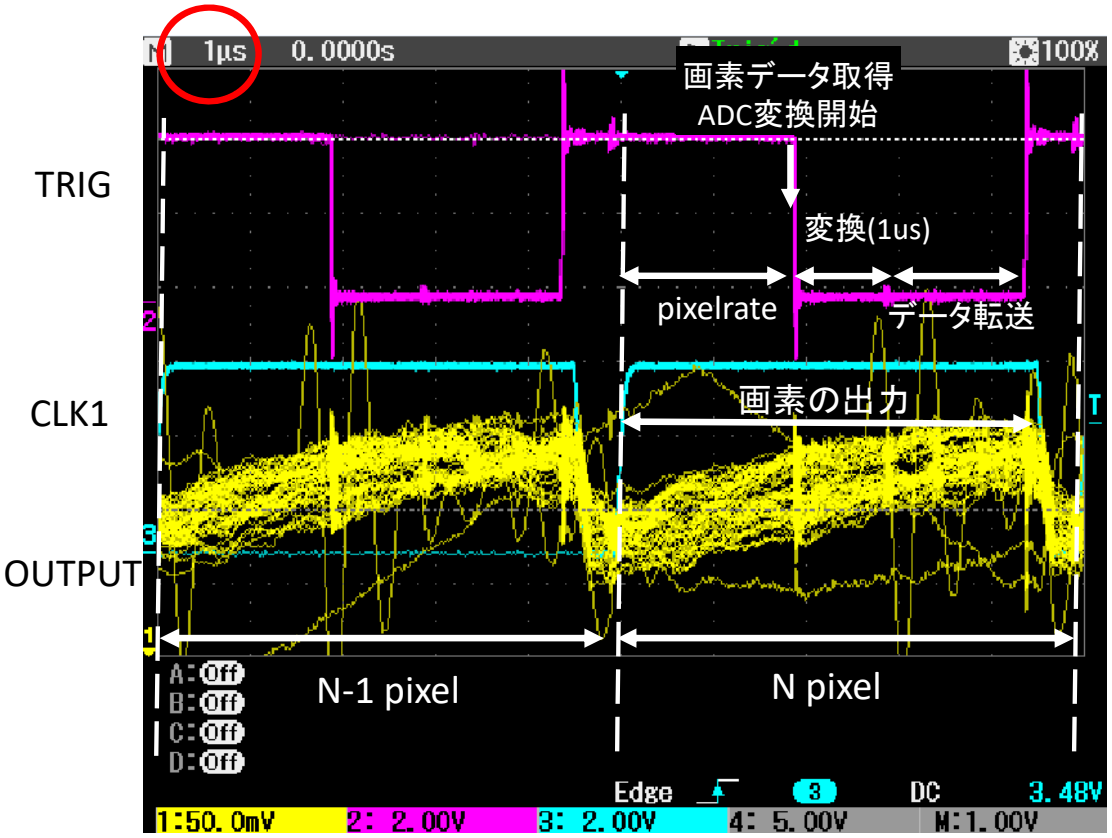


32チャネル読み出し

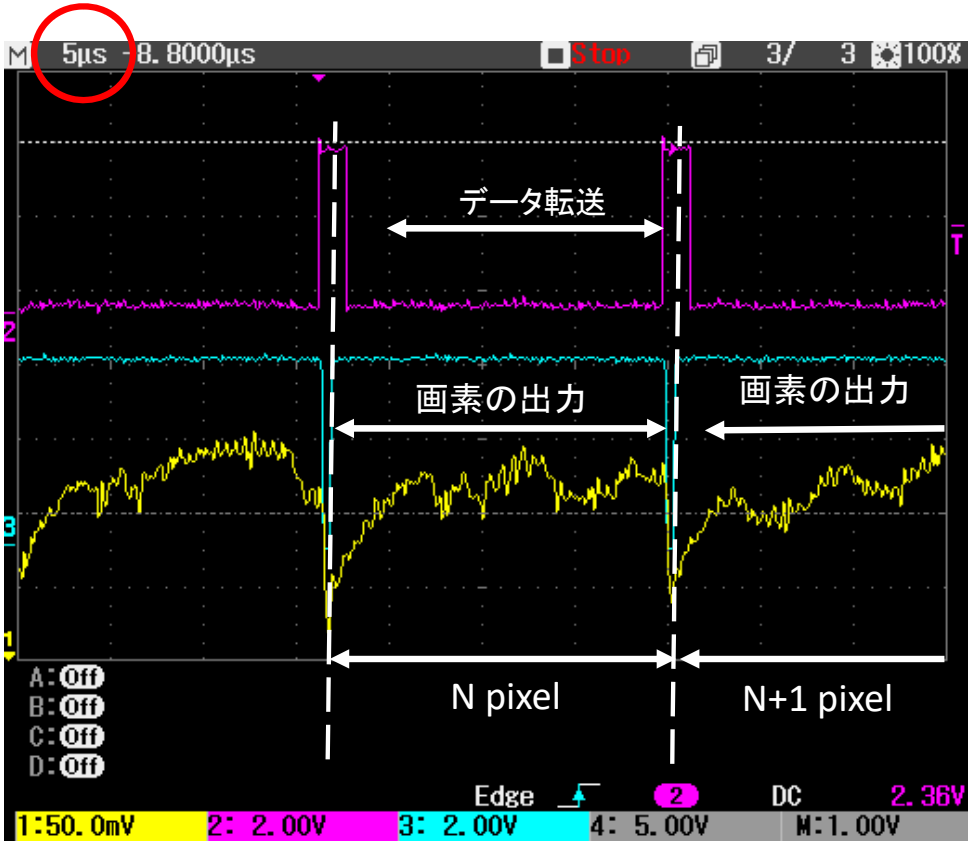


読み出しのタイミング

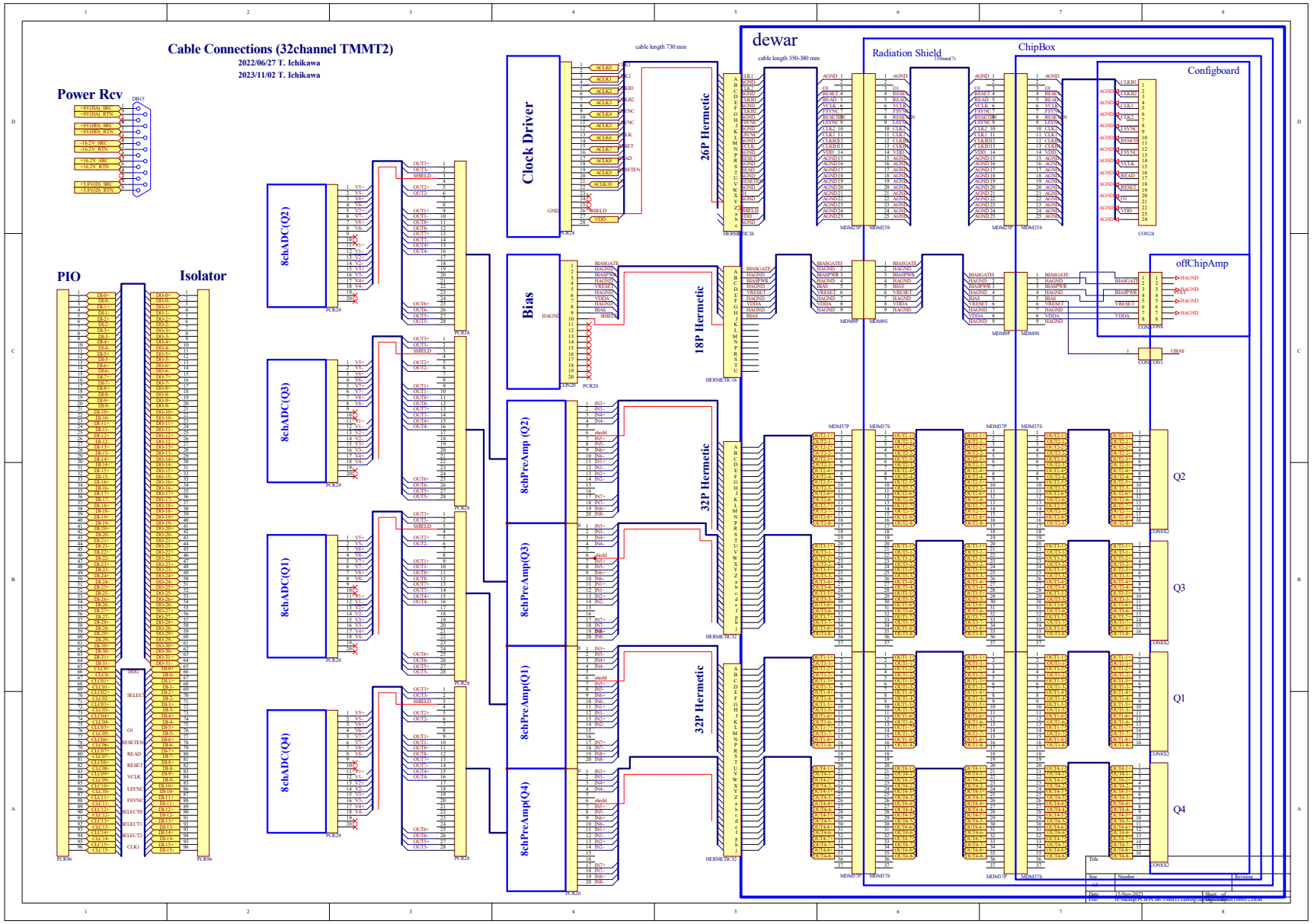
4チャネル読み出し



32チャネル読み出し

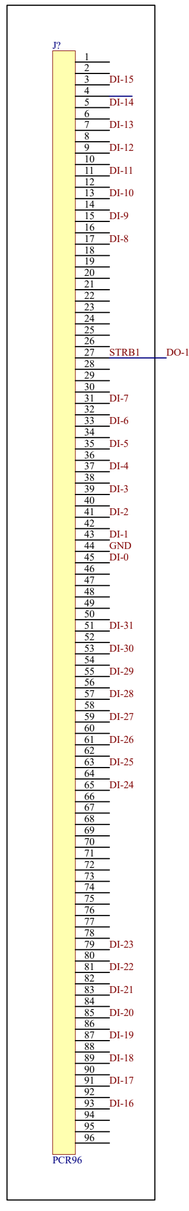


データバス太さの制限で、読み出しに時間がかかる

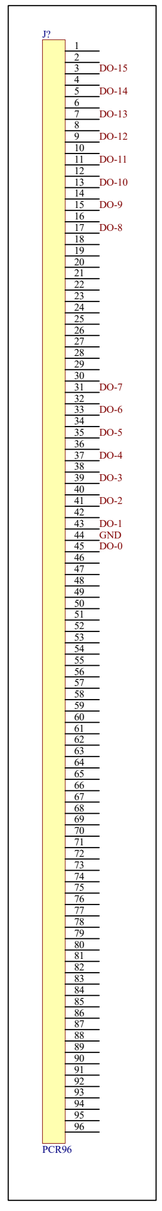

Cable Connections (32channel TMMT2)
2022/06/27 T. Ichikawa
2023/11/02 T. Ichikawa
Power Rcv
PIO
Isolator
dewar
cable length 730 mm
cable length 350-380 mm
Radiation Shield
ChipBox
Configboard
offChipAmp
Clock Driver
Bias
8chADC(Q2)
8chADC(Q3)
8chADC(Q1)
8chADC(Q4)
8chPreAmp (Q2)
8chPreAmp(Q3)
8chPreAmp(Q1)
8chPreAmp(Q4)
26P Hermetic
18P Hermetic
32P Hermetic
32P Hermetic
Q2
Q3
Q1
Q4
Title
Size
Number
Revision
Date
File

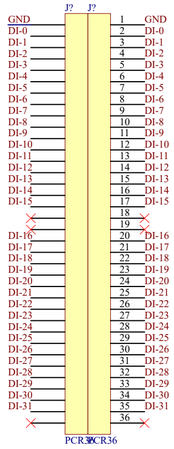
2014/09/01 (T. Ichikawa)

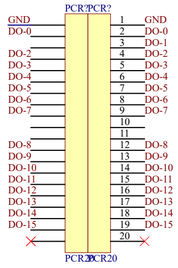
PCI2772 (IN)



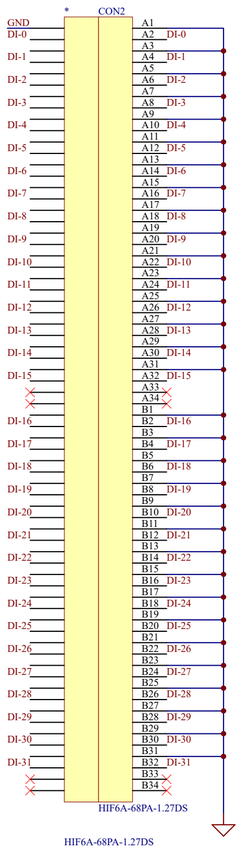
PCI2772 (OUT)



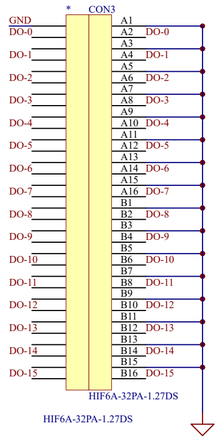




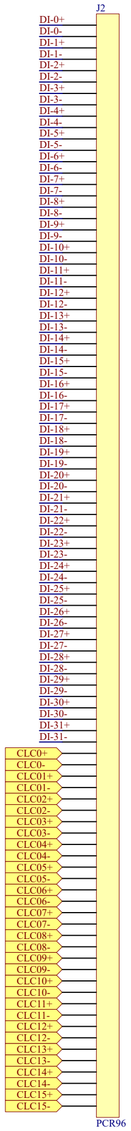
Isolation PIOV3



HIF6A-68PA-1.27DS



HIF6A-32PA-1.27DS

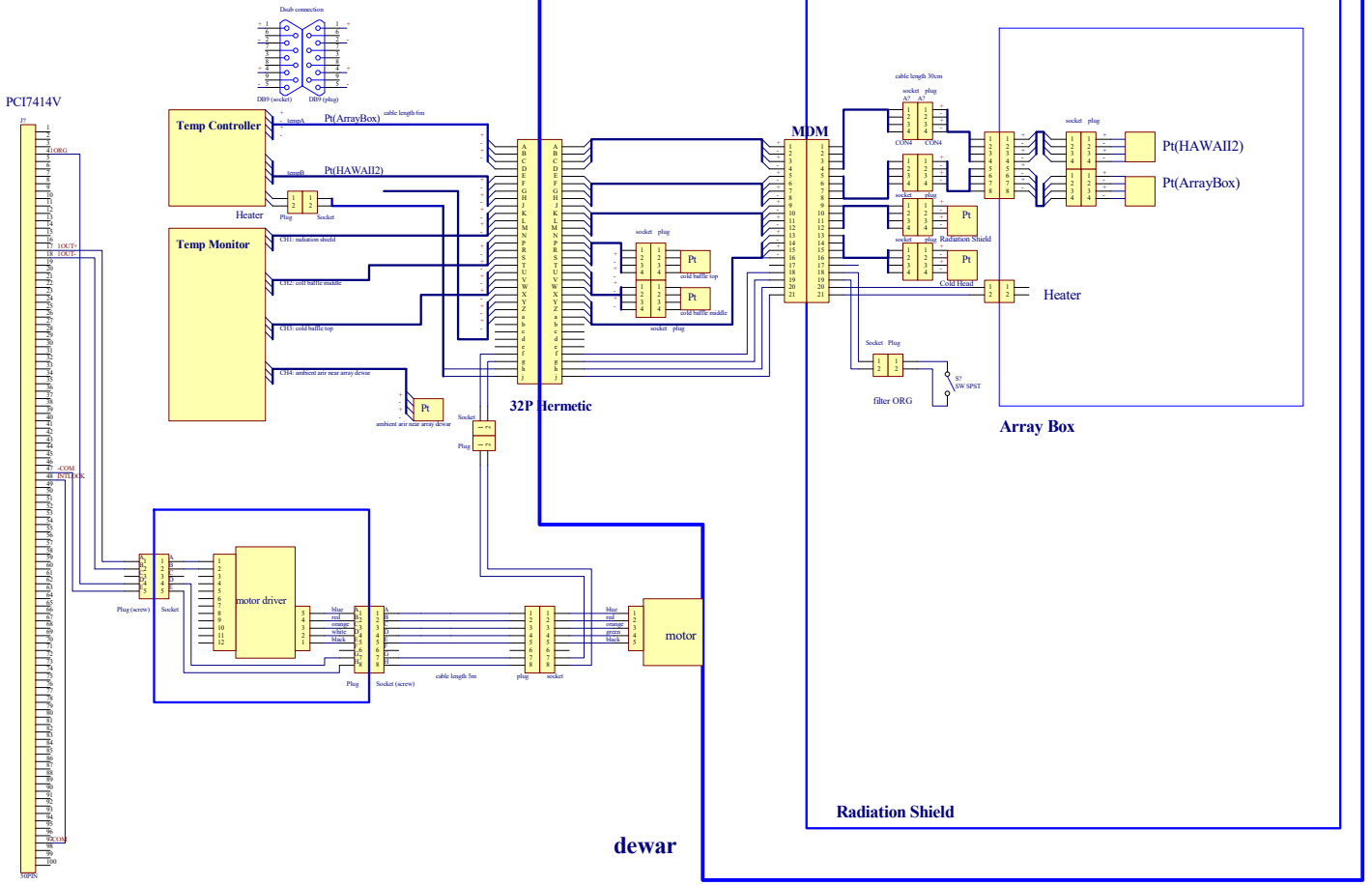


TACS

Title			
Size A2	Number		Revision
Date:	2021/08/11		Sheet of
File:	G:\backup\..\PIOV3cabling.sch		Drawn By:

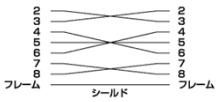
Cable Connections for temerature monitor (TMMT2)

2023/10/10 T. Ichikawa



Title		
Size: A2	Number	Revision
Date: 10-Oct-2023	Sheet of	
File: H:\PCB\TMMT2-cabling\Cabling\tempera.ddb	Drawn By:	

コントロールラックーTMMT2間のケーブル長



インターリンクケーブル　TMMT用

RS232C

AC100V

Power
TEXIO

70cm(?)

RS232C
RS232C
RS232C

PC
（インターフェス社
FAコントローラ）

96線信号ケーブル

8m （TMMT用）

TACS

1m

73cm

モーター(5芯)フィルター(2芯)

Motor Driver
(Melec GD5410)

7.5m

TONIC3

Pt センサー(4芯×3)

RS232C

Temperature
Controlle
(LakeShore M331)

ヒーター(2芯)

0.5m

5.5m

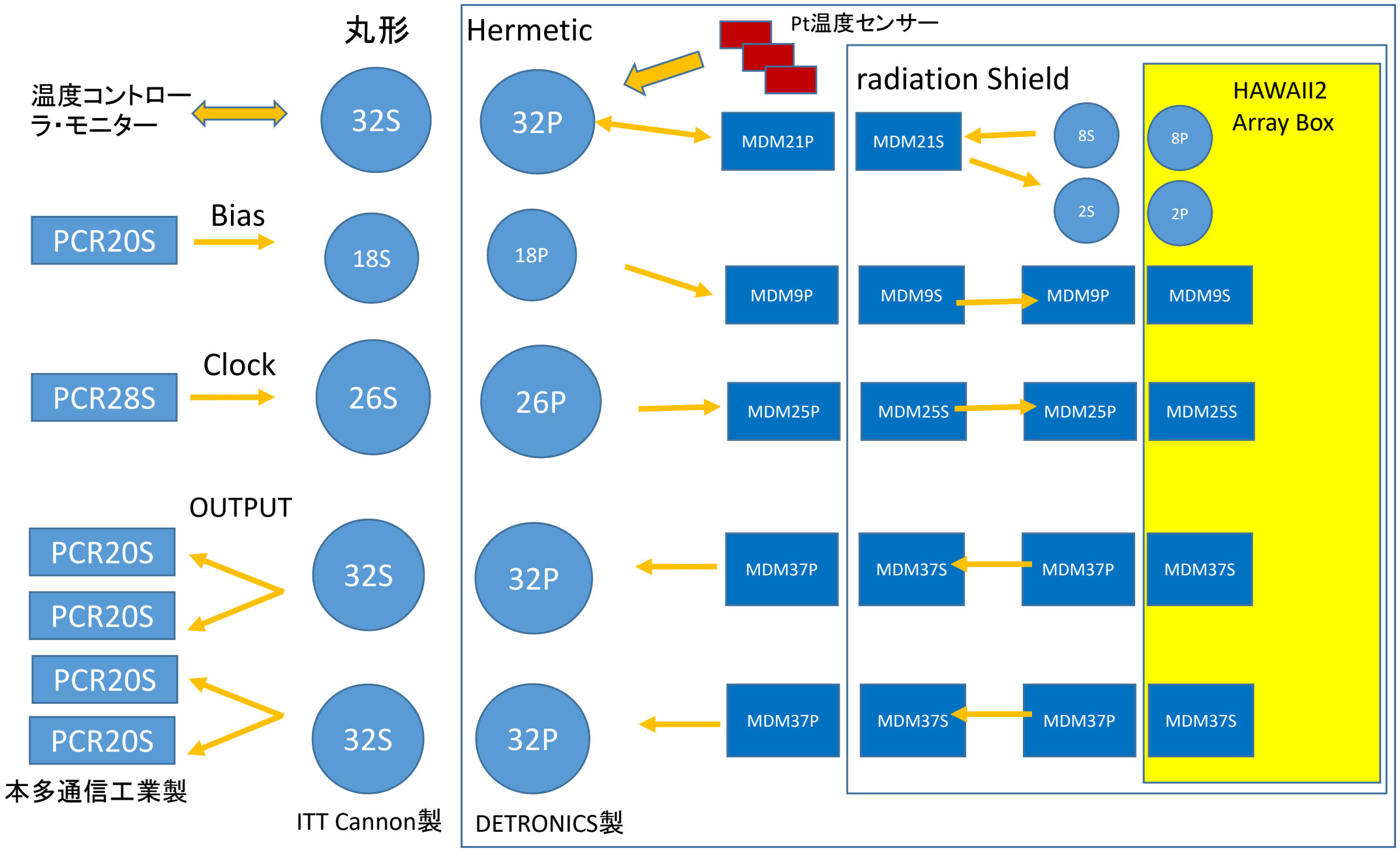
Pt センサー(4芯×4)

RS232C

Temperature
Monitor
(理化工業　MA900)

HAWAII2 in TONIC3　配線

2022/12/17　市川



Back Plane

DIN1

A1	1	DAT1-0	
A2	2	DAT1-1	
A3	3	DAT1-2	
A4	4	DAT1-3	Digitized Data (Quad1)
A5	5	DAT1-4	
A6	6	DAT1-5	
A7	7	DAT1-6	
A8	8	DAT1-7	
A9	9	DAT1-8	
A10	10	DAT1-9	
A11	11	DAT1-10	
A12	12	DAT1-11	
A13	13	DAT1-12	
A14	14	DAT1-13	
A15	15	DAT1-14	
A16	16	DAT1-15	
A17	17	DAT2-0	
A18	18	DAT2-1	
A19	19	DAT2-2	
A20	20	DAT2-3	Digitized Data (Quad 2)
A21	21	DAT2-4	
A22	22	DAT2-5	
A23	23	DAT2-6	
A24	24	DAT2-7	
A25	25	DAT2-8	
A26	26	DAT2-9	
A27	27	DAT2-10	
A28	28	DAT2-11	
A29	29	DAT2-12	
A30	30	DAT2-13	
A31	31	DAT2-14	
A32	32	DAT2-15	
B1	33	DAT3-0	
B2	34	DAT3-1	
B3	35	DAT3-2	
B4	36	DAT3-3	Digitized Data (Quad3)
B5	37	DAT3-4	
B6	38	DAT3-5	
B7	39	DAT3-6	
B8	40	DAT3-7	
B9	41	DAT3-8	
B10	42	DAT3-9	
B11	43	DAT3-10	
B12	44	DAT3-11	
B13	45	DAT3-12	
B14	46	DAT3-13	
B15	47	DAT3-14	
B16	48	DAT3-15	
B17	49	DAT4-0	
B18	50	DAT4-1	
B19	51	DAT4-2	
B20	52	DAT4-3	Digitized Data (Quad 3)
B21	53	DAT4-4	
B22	54	DAT4-5	
B23	55	DAT4-6	
B24	56	DAT4-7	
B25	57	DAT4-8	
B26	58	DAT4-9	
B27	59	DAT4-10	
B28	60	DAT4-11	
B29	61	DAT4-12	
B30	62	DAT4-13	
B31	63	DAT4-14	
B32	64	DAT4-15	
C1	65	CLK0	TRIG ADC Trigger
C2	66	CLK1	
C3	67	CLK2	SELECT BUS(A,B)Select
C4	68	CLK3	
C5	69	CLK4	
C6	70	CLK5	O1
C7	71	CLK6	RESETEN
C8	72	CLK7	READ
C9	73	CLK8	RESET
C10	74	CLK9	VCLK
C11	75	CLK10	LSYNC
C12	76	CLK11	FSYNC
C13	77	CLK12	Octagon Select
C14	78	CLK13	Octagon Select
C15	79	CLK14	Octagon Select
C16	80	CLK15	CLK1
C17	81		
C18	82		
C19	83		
C20	84		
C21	85	DGND	Digital Ground
C22	86	Vcc	Digital Power (5V)
C23	87	DGND	Digital Ground
C24	88	AGND	Analog Ground
C25	89	+15V	Analog +15V
C26	90	AGND	Analog Ground
C27	91	-15V	Analog -15V
C28	92	AGND	Analog Ground Analog Ground = HAWAII2 Clock Ground
C29	93	+8.0V(HD)	HAWAII2 VDD
C30	94	HAGND	HAWAII2 Analog Ground
C31	95	+7.0V(HA)	HAWAII2 Power
C32	96	HAGND	HAWAII2 Ground

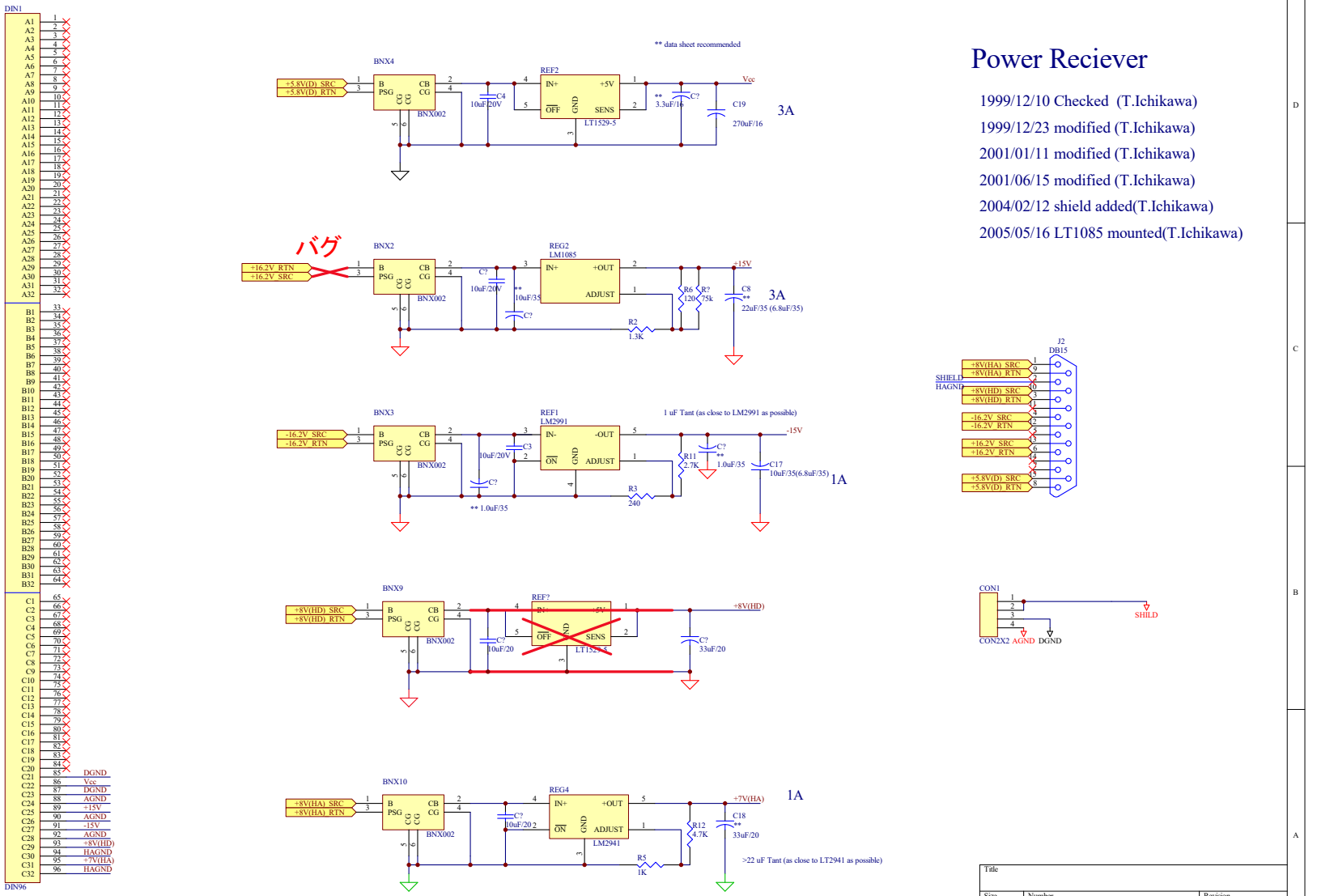
DIN96

2000/11/03 T. Ichikawa
2000/12/31 T. Ichikawa
2004/10/12 T. Ichikawa
2005/01/04 T. Ichikawa

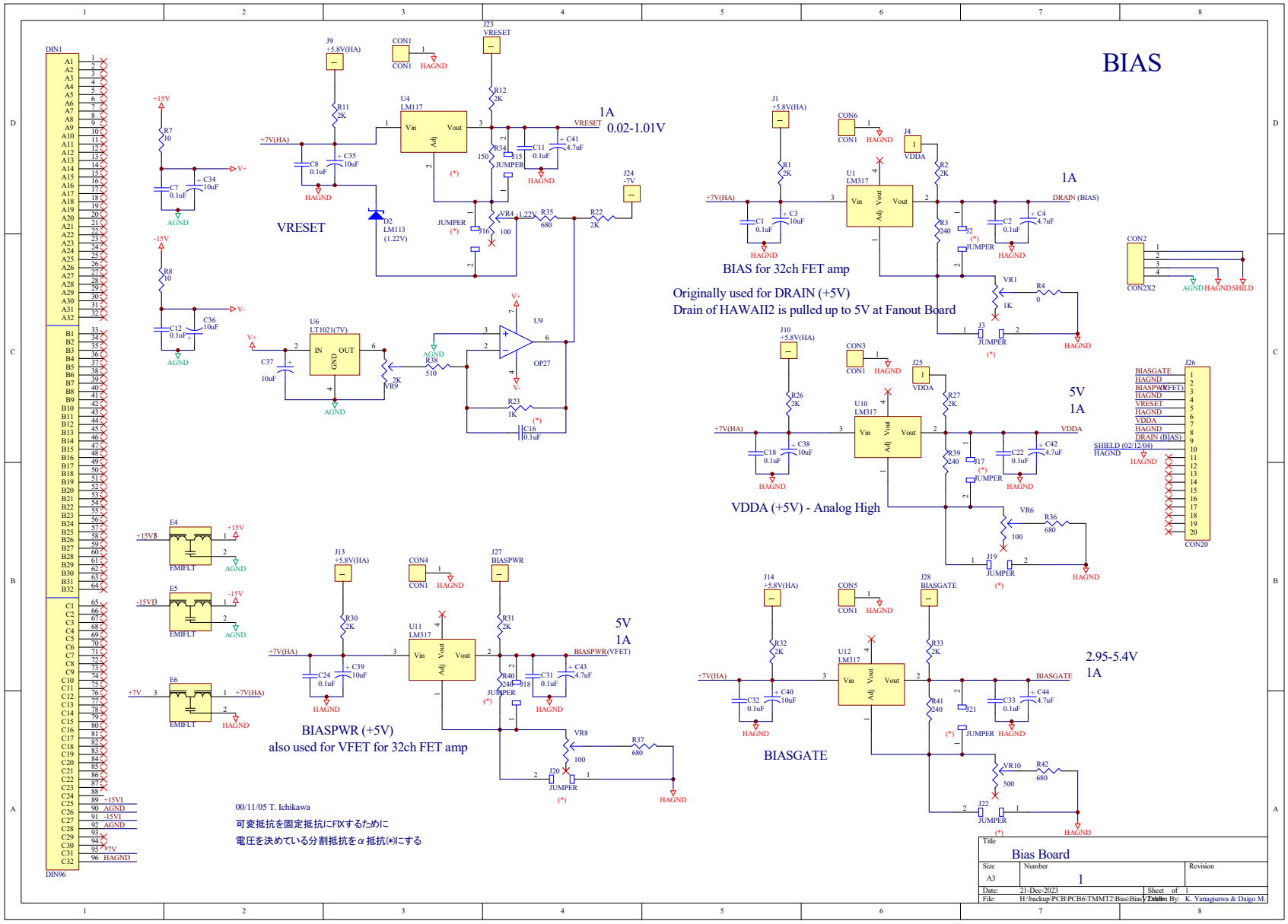
Title			
Size A4	Number		Revision
Date:	4-Jan-2005	Sheet of	
File:	F:\HAWAII2PCB\BackPlane\BackPlaneV2.ddb	Drawn By:	

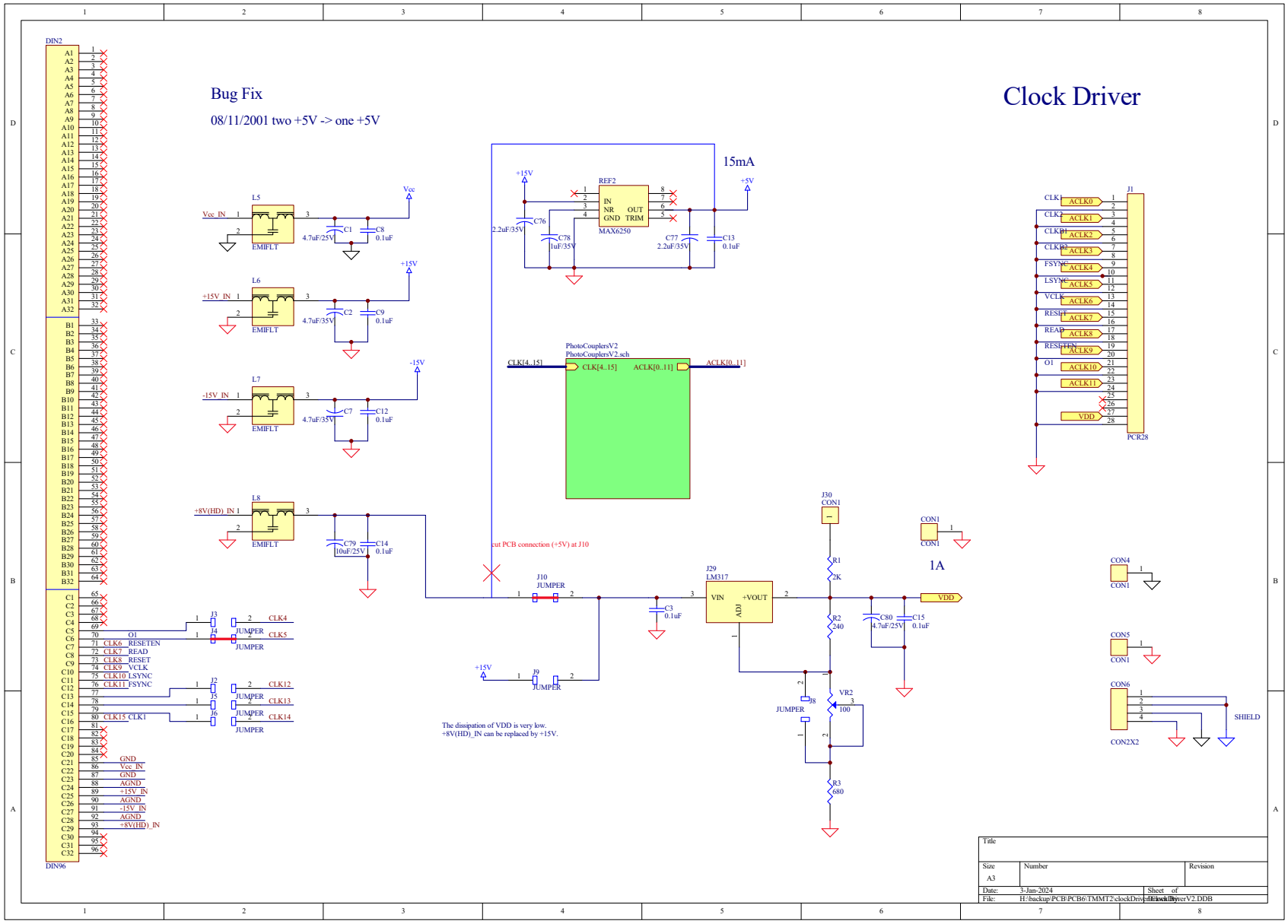
Power Reciever

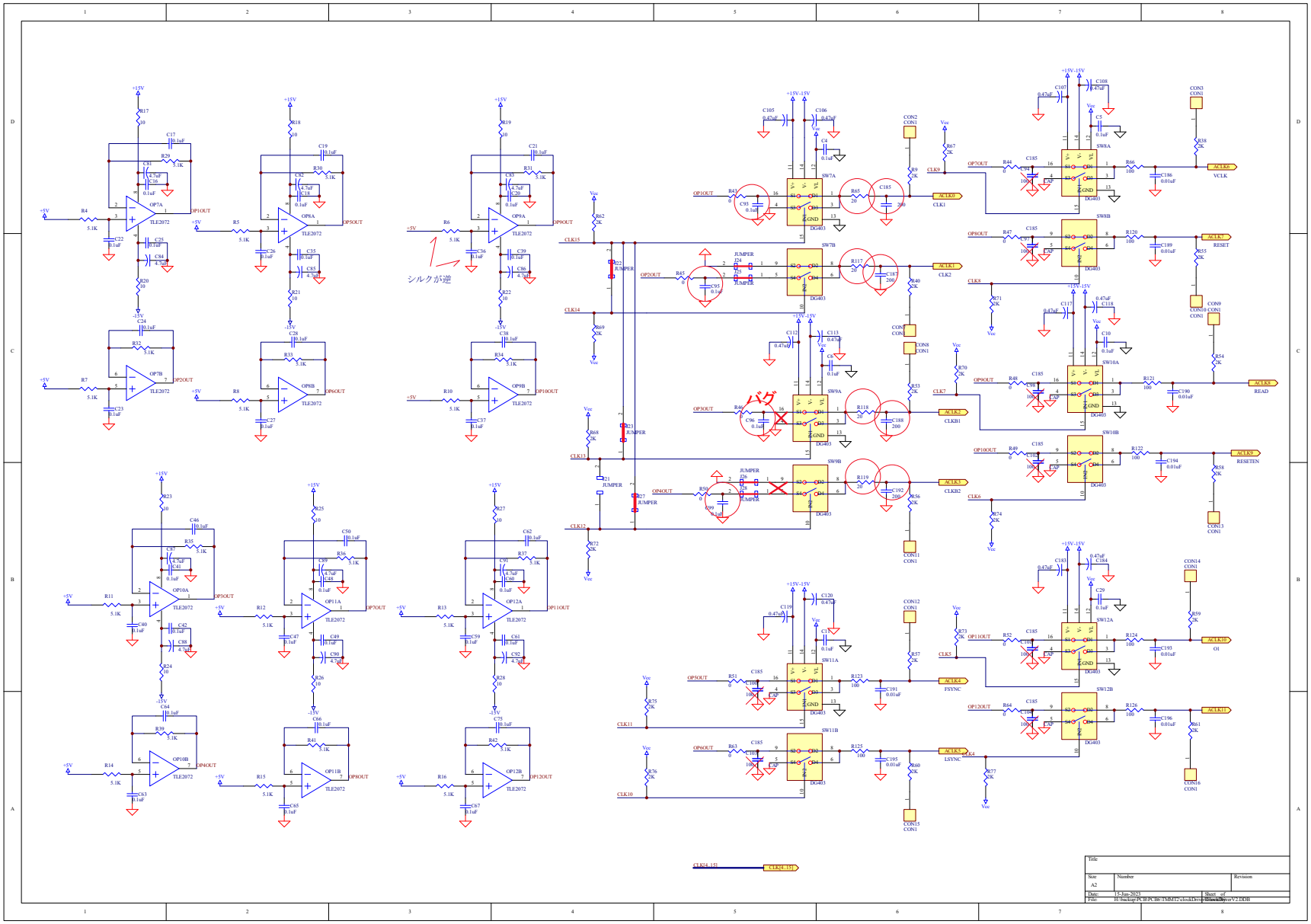
1999/12/10 Checked (T.Ichikawa)
1999/12/23 modified (T.Ichikawa)
2001/01/11 modified (T.Ichikawa)
2001/06/15 modified (T.Ichikawa)
2004/02/12 shield added(T.Ichikawa)
2005/05/16 LT1085 mounted(T.Ichikawa)

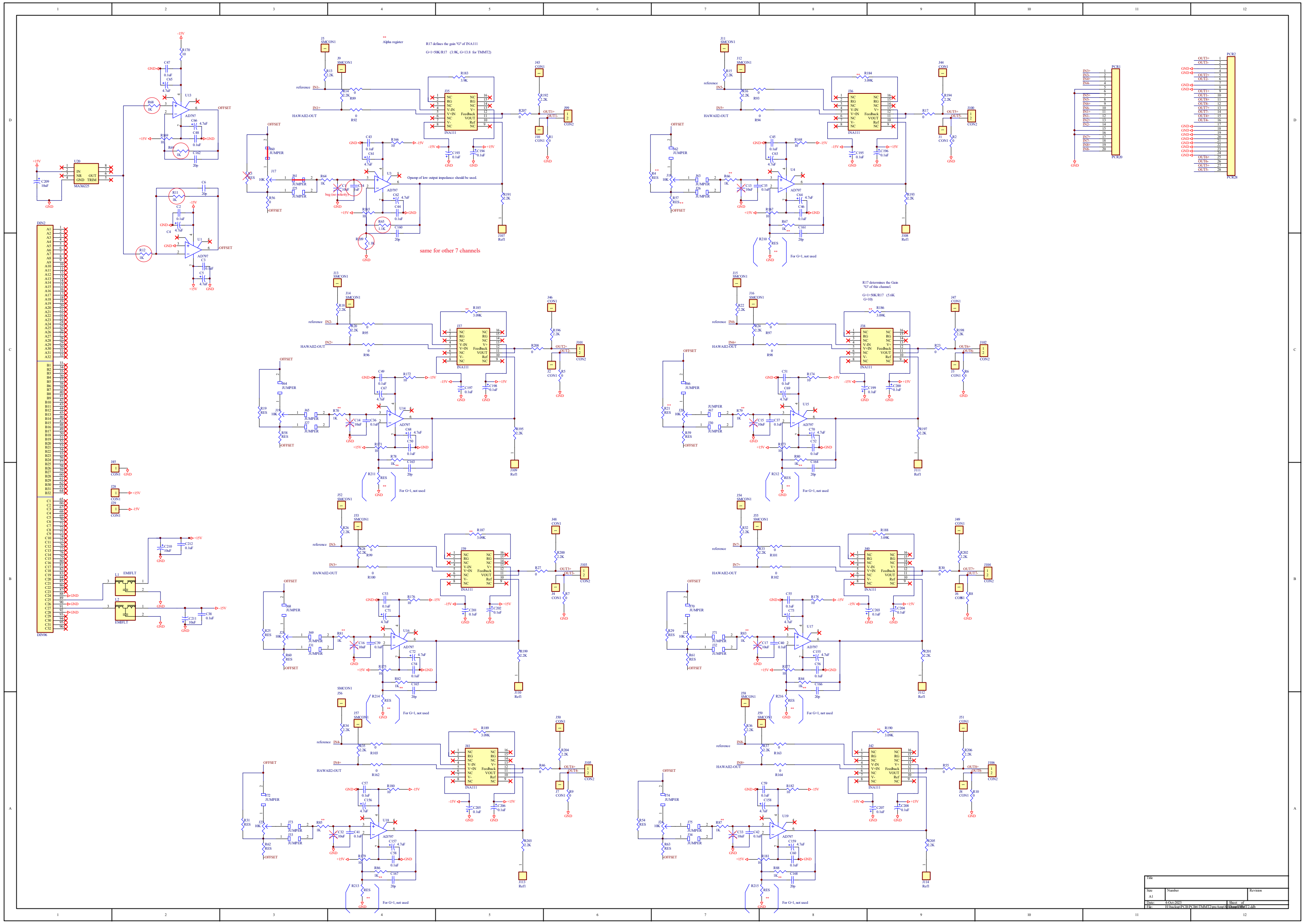


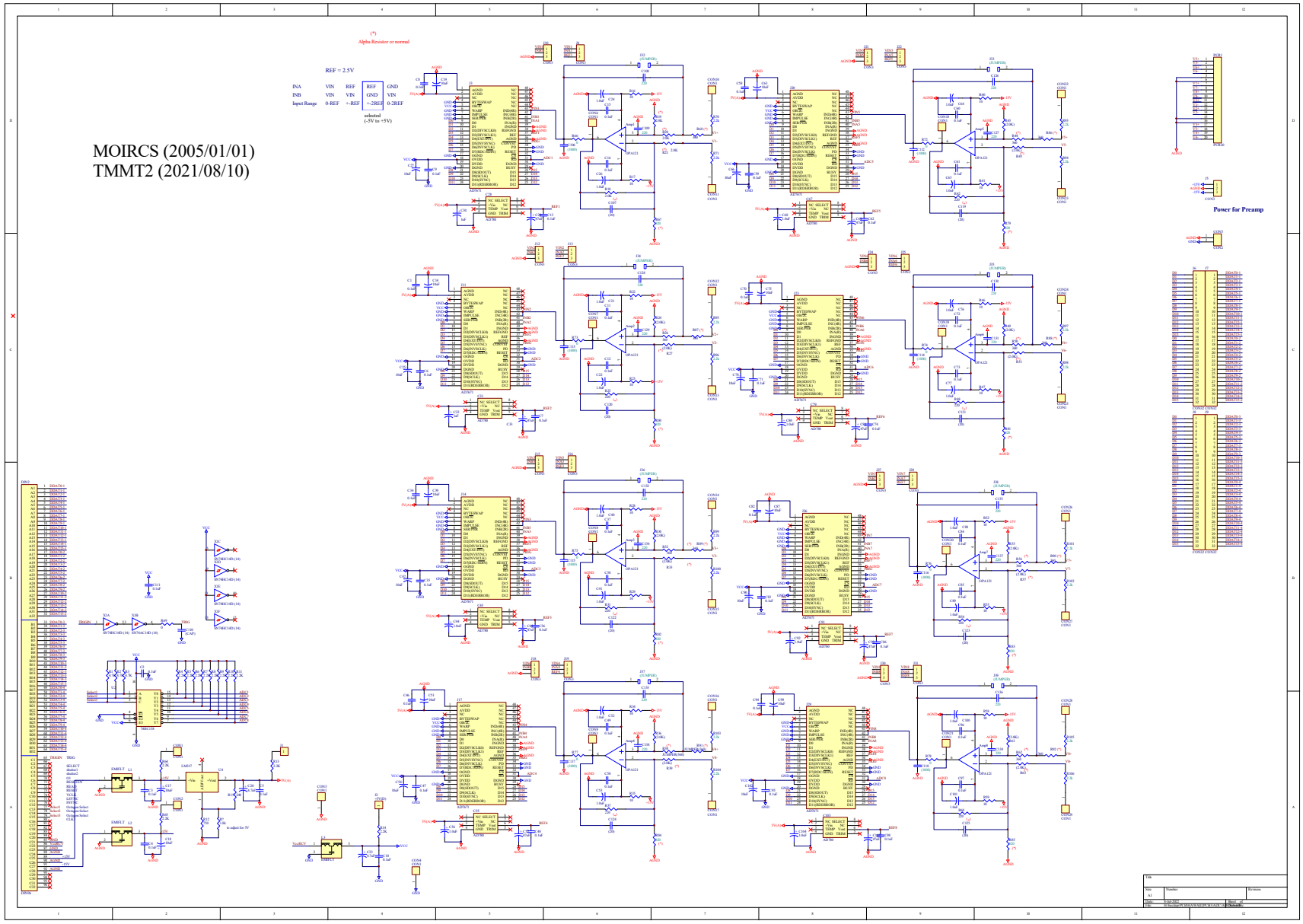
Title		
Size A3	Number	Revision
Date: 15-Dec-2022	Sheet of	
File: H:\PCB6\TMMT2\powerRcv\PowerRcvV2.ddb	Drawn By:	


BIAS
VRESET
1A
0.02-1.01V
BIAS for 32ch FET amp
Originally used for DRAIN (+5V)
Drain of HAWAII2 is pulled up to 5V at Fanout Board
1A
5V
1A
VDDA (+5V) - Analog High
BIASPWR (+5V)
also used for VFET for 32ch FET amp
5V
1A
2.95-5.4V
1A
BIASGATE
00/11/05 T. Ichikawa
可変抵抗を固定抵抗にFIXするために
電圧を決めている分割抵抗をα抵抗(*)にする
Title
Bias Board
Size
A3
Number
1
Revision
Date:
21-Dec-2023
Sheet of
1
File:
H:\backup\PCB\PCB6\TMMT2\Bias\Bias7.ddb
Drawn By:
K. Yanagisawa & Daigo M.


Bug Fix
08/11/2001 two +5V -> one +5V
Clock Driver
15mA
1A
DIN2
DIN96
L5
L6
L7
L8
EMIFLT
4.7uF/25V
4.7uF/35V
0.1uF
10uF/25V
Vcc
Vcc_IN
+15V_IN
-15V_IN
+8V(HD)_IN
REF2
MAX6250
IN
NR
OUT
GND
TRIM
2.2uF/35V
1uF/35V
+5V
PhotoCouplersV2
PhotoCouplersV2.sch
CLK[4..15]
ACLK[0..11]
cut PCB connection (+5V) at J10
J10
JUMPER
J29
LM317
VIN
+VOUT
ADJ
J30
CON1
R1
2K
R2
240
VR2
100
R3
680
J8
J9
C3
C80
C15
VDD
J1
PCR28
ACLK0
ACLK1
ACLK2
ACLK3
ACLK4
ACLK5
ACLK6
ACLK7
ACLK8
ACLK9
ACLK10
ACLK11
CLK1
CLK2
CLKB1
CLKB2
FSYNC
LSYNC
VCLK
RESET
READ
RESETEN
O1
VDD
CON4
CON5
CON6
CON2X2
SHIELD
J2
J3
J4
J5
J6
CLK4
CLK5
CLK6_RESETEN
CLK7_READ
CLK8_RESET
CLK9_VCLK
CLK10_LSYNC
CLK11_FSYNC
CLK12
CLK13
CLK14
CLK15_CLK1
GND
AGND
The dissipation of VDD is very low.
+8V(HD)_IN can be replaced by +15V.
Title
Size
A3
Number
Revision
Date: 3-Jan-2024
Sheet of
File: H:\backup\PCB\PCB6\TMMT2\clockDriverV2.DDB


シルクが逆
バグ
CLK[4..15]
Title
Size: A2
Number
Revision
Date: 15-Jan-2023
Sheet of
File: H:\backup\PCB\PCB6\TMM12-clockDown\Block\Down V2.DDB

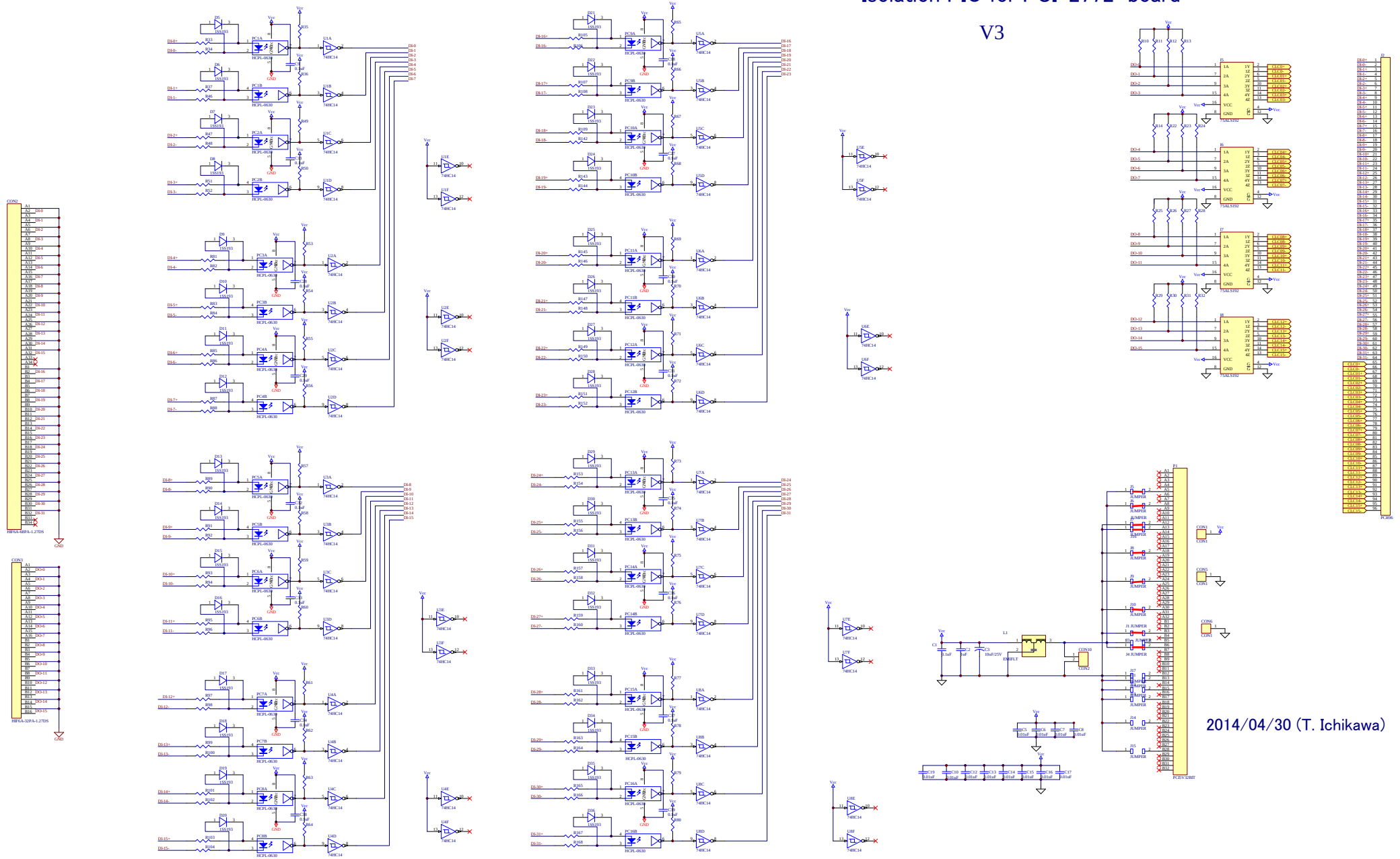

same for other 7 channels


MOIRCS (2005/01/01)
TMMT2 (2021/08/10)
(*)
Alpha Resistor or normal
REF = 2.5V
INA VIN REF REF GND
INB VIN VIN GND VIN
Input Range 0-REF +-REF +-2REF 0-2REF
selected
(-5V to +5V)
Power for Preamp

56Ω for photocoupler

Isolation PIO for PCI-2772 board

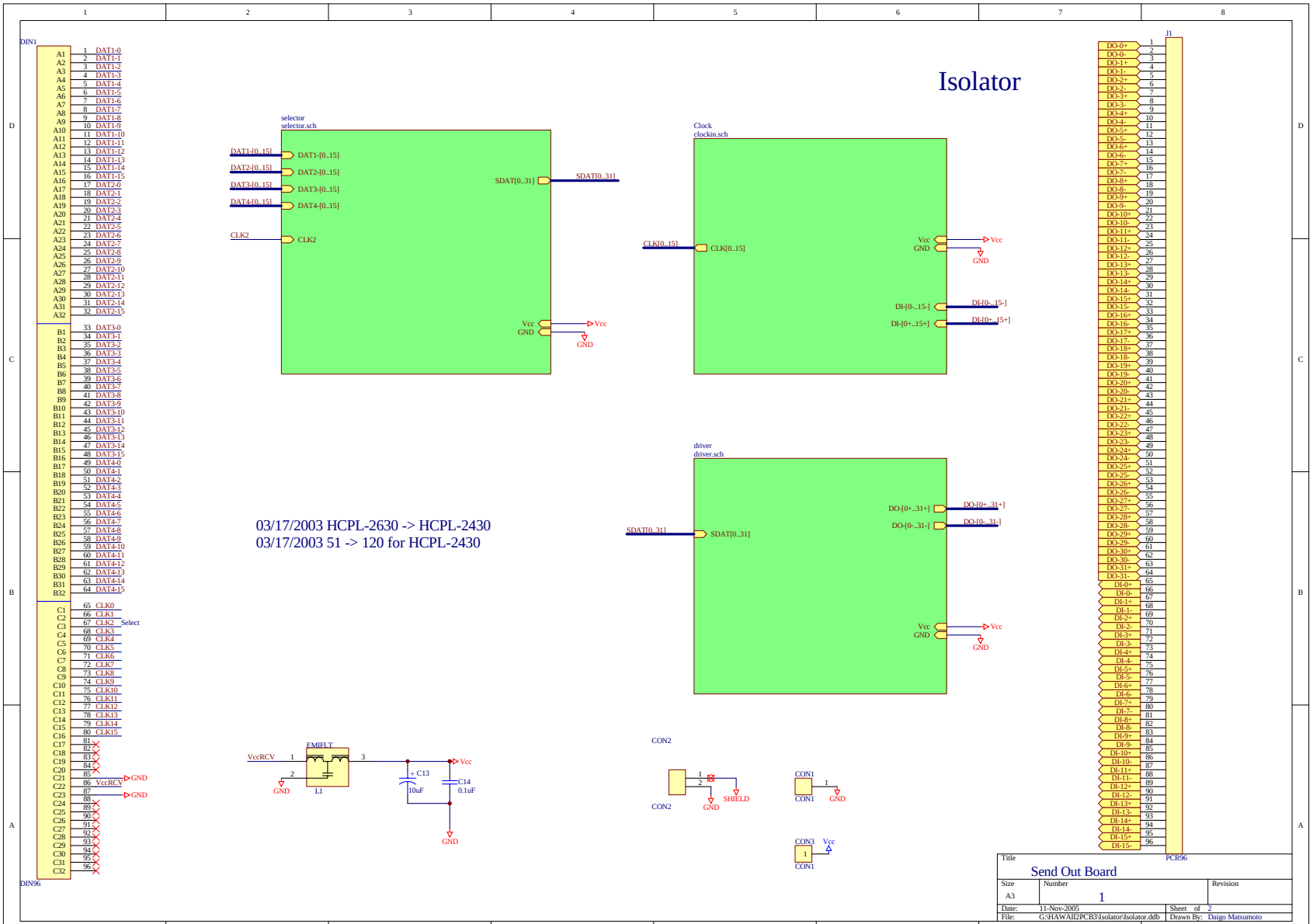
V3



2014/04/30 (T. Ichikawa)

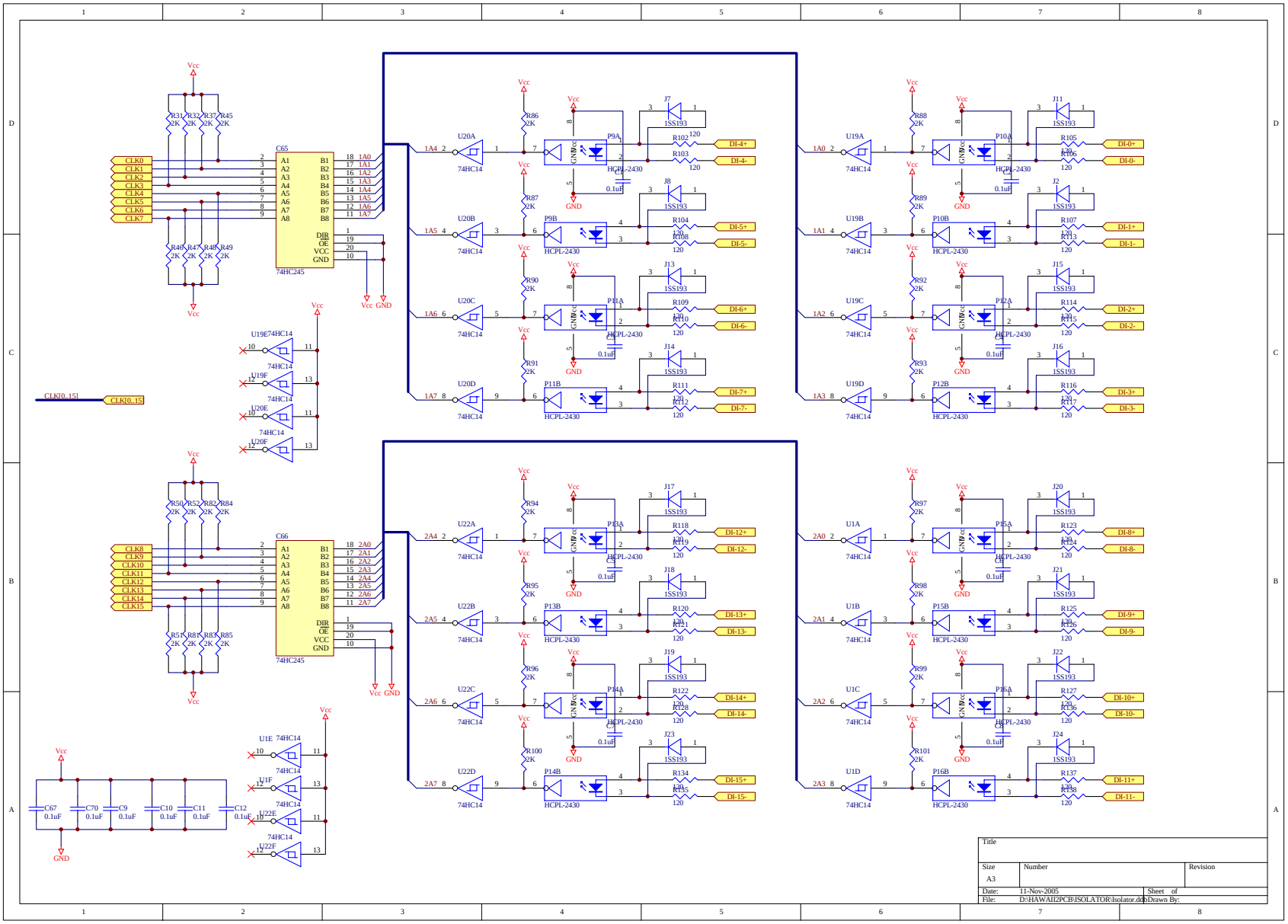
Title		
Size: A1	Number	Revision
Date: 2015/05/10	Sheet of	
File: I:\PCI\PCI-PIO\Documents\PIO\V3.sch	Drawn By:	

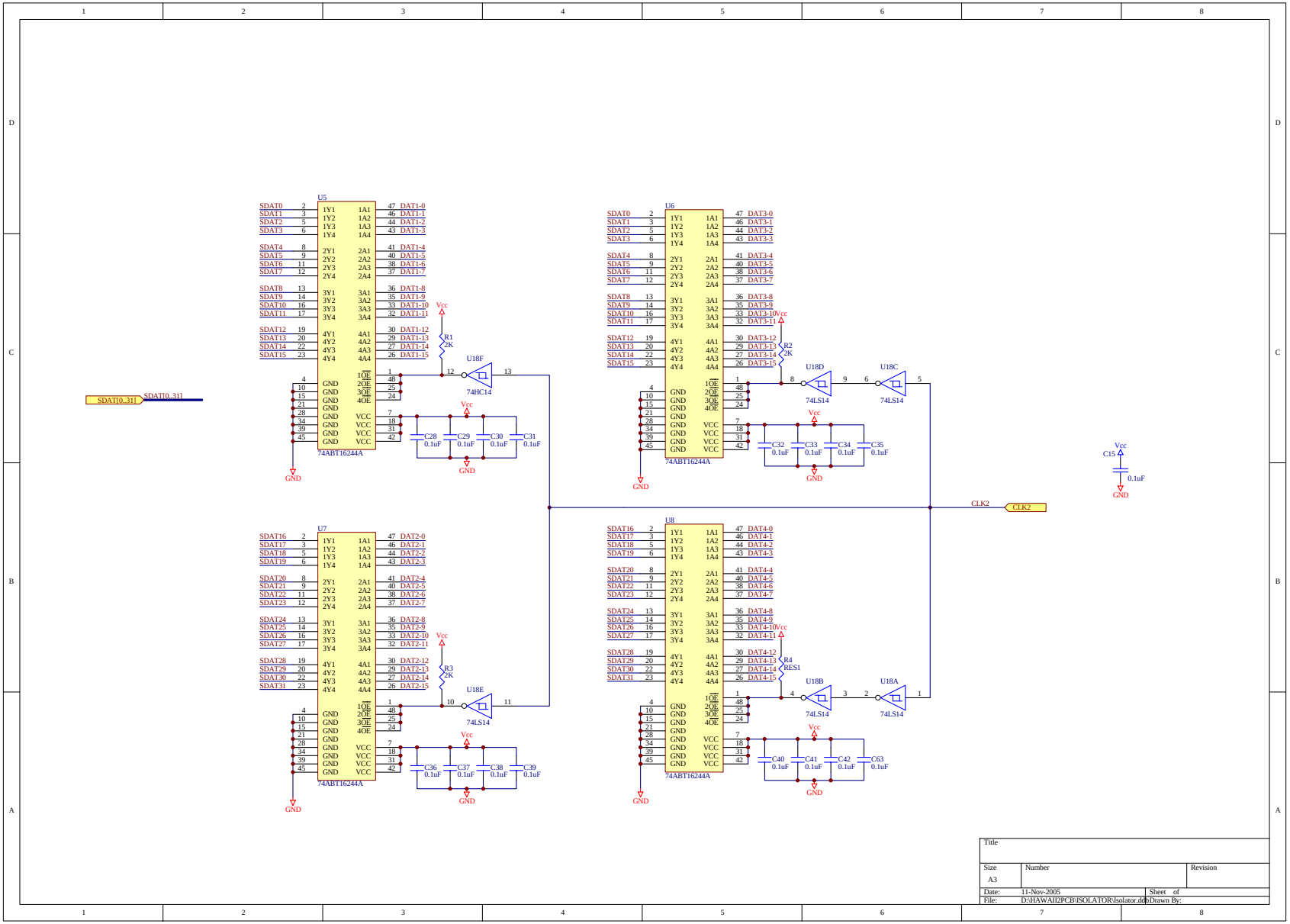
Isolator



03/17/2003 HCPL-2630 -> HCPL-2430
03/17/2003 51 -> 120 for HCPL-2430

Title	Send Out Board		
Size: A3	Number: 1		Revision:
Date: 11-Nov-2005		Sheet of 2	
File: G:\HAWAII2PCB3\Isolator\Isolator.ddb		Drawn By: Daigo Matsumoto	

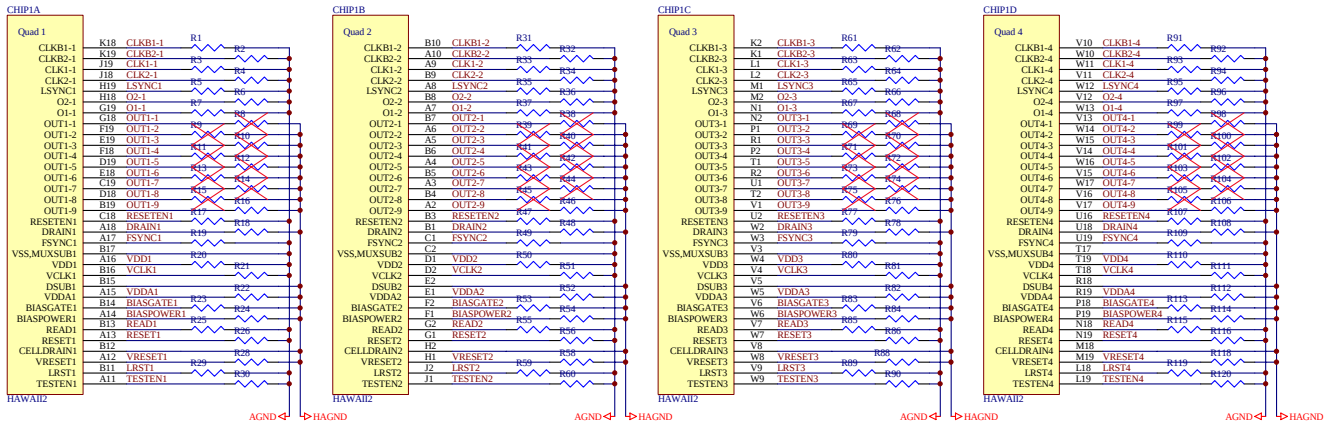

CLK[0..15]
74HC245
74HC14
HCPL-2430
1SS193
Vcc
GND
DI-0+
DI-0-
DI-1+
DI-1-
DI-2+
DI-2-
DI-3+
DI-3-
DI-4+
DI-4-
DI-5+
DI-5-
DI-6+
DI-6-
DI-7+
DI-7-
DI-8+
DI-8-
DI-9+
DI-9-
DI-10+
DI-10-
DI-11+
DI-11-
DI-12+
DI-12-
DI-13+
DI-13-
DI-14+
DI-14-
DI-15+
DI-15-
Title
Size
A3
Number
Revision
Date:
11-Nov-2005
Sheet of
File:
D:\HAWAII2PCB\ISOLATOR\Isolator.ddb
Drawn By:

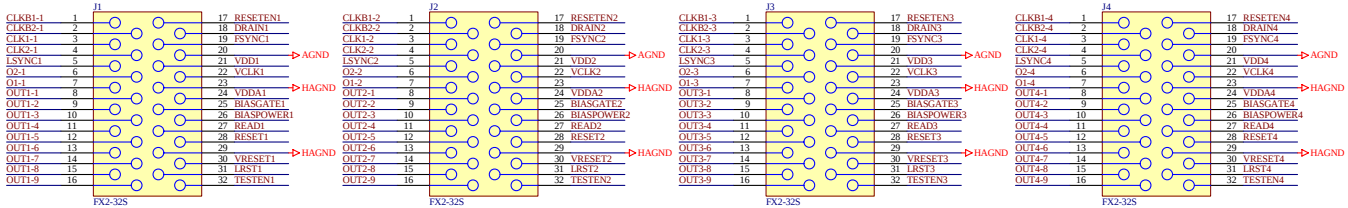

SDAT[0..31]
SDAT[0..31]
U5
SDAT0 SDAT1 SDAT2 SDAT3 SDAT4 SDAT5 SDAT6 SDAT7 SDAT8 SDAT9 SDAT10 SDAT11 SDAT12 SDAT13 SDAT14 SDAT15
DAT1-0 DAT1-1 DAT1-2 DAT1-3 DAT1-4 DAT1-5 DAT1-6 DAT1-7 DAT1-8 DAT1-9 DAT1-10 DAT1-11 DAT1-12 DAT1-13 DAT1-14 DAT1-15
74ABT16244A
Vcc
R1 2K
U18F
74HC14
C28 C29 C30 C31 0.1uF
GND
U6
SDAT0 SDAT1 SDAT2 SDAT3 SDAT4 SDAT5 SDAT6 SDAT7 SDAT8 SDAT9 SDAT10 SDAT11 SDAT12 SDAT13 SDAT14 SDAT15
DAT3-0 DAT3-1 DAT3-2 DAT3-3 DAT3-4 DAT3-5 DAT3-6 DAT3-7 DAT3-8 DAT3-9 DAT3-10 DAT3-11 DAT3-12 DAT3-13 DAT3-14 DAT3-15
74ABT16244A
R2 2K
U18D
U18C
74LS14
C32 C33 C34 C35 0.1uF
C15
0.1uF
CLK2
U7
SDAT16 SDAT17 SDAT18 SDAT19 SDAT20 SDAT21 SDAT22 SDAT23 SDAT24 SDAT25 SDAT26 SDAT27 SDAT28 SDAT29 SDAT30 SDAT31
DAT2-0 DAT2-1 DAT2-2 DAT2-3 DAT2-4 DAT2-5 DAT2-6 DAT2-7 DAT2-8 DAT2-9 DAT2-10 DAT2-11 DAT2-12 DAT2-13 DAT2-14 DAT2-15
74ABT16244A
R3 2K
U18E
74LS14
C36 C37 C38 C39 0.1uF
U8
SDAT16 SDAT17 SDAT18 SDAT19 SDAT20 SDAT21 SDAT22 SDAT23 SDAT24 SDAT25 SDAT26 SDAT27 SDAT28 SDAT29 SDAT30 SDAT31
DAT4-0 DAT4-1 DAT4-2 DAT4-3 DAT4-4 DAT4-5 DAT4-6 DAT4-7 DAT4-8 DAT4-9 DAT4-10 DAT4-11 DAT4-12 DAT4-13 DAT4-14 DAT4-15
74ABT16244A
R4 RES1
U18B
U18A
74LS14
C40 C41 C42 C63 0.1uF
Title
Size A3
Number
Revision
Date: 11-Nov-2005
Sheet of
File: D:\HAWAII2PCB\ISOLATOR\Isolator.ddb
Drawn By:

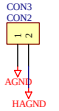
Title: Send Out Board		
Size: A3	Number: 2	Revision:
Date: 11-Nov-2005	Sheet of 2	
File: D:\HAWAII2PCB\ISOLATOR\Isolator.ddb	Drawn By: Daigo Matsumoto	

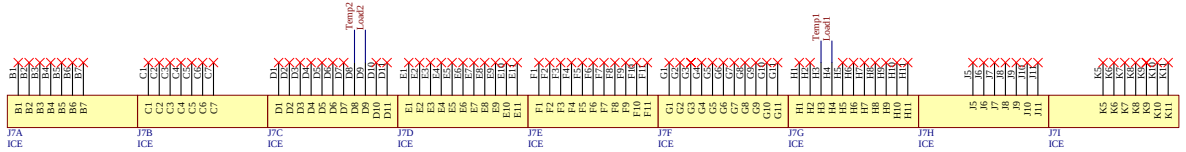
Resistors (R1,R2,R3,...,R120) : 10M Ohm.

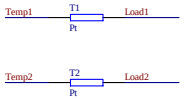
Fanout for HAWAII2







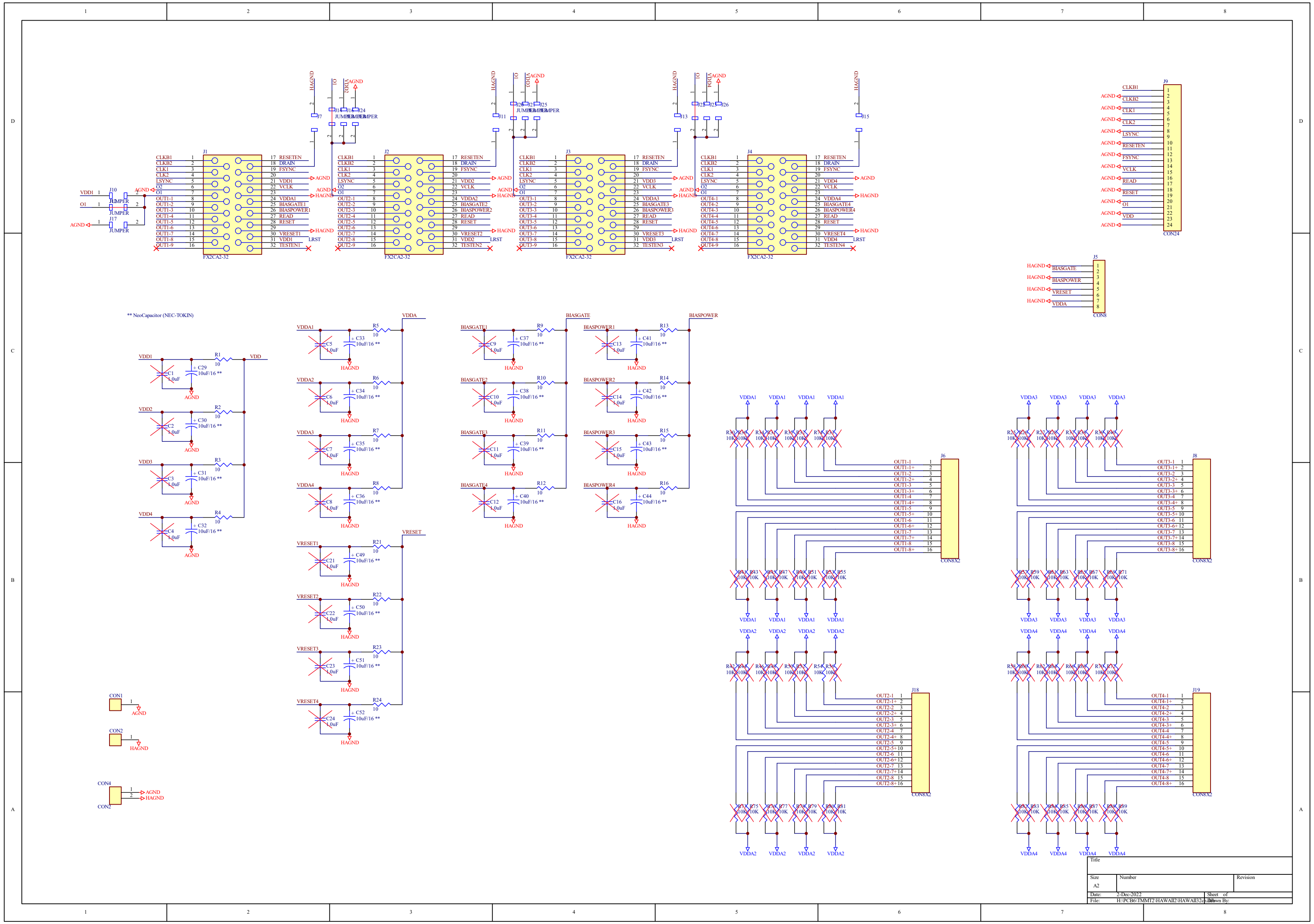




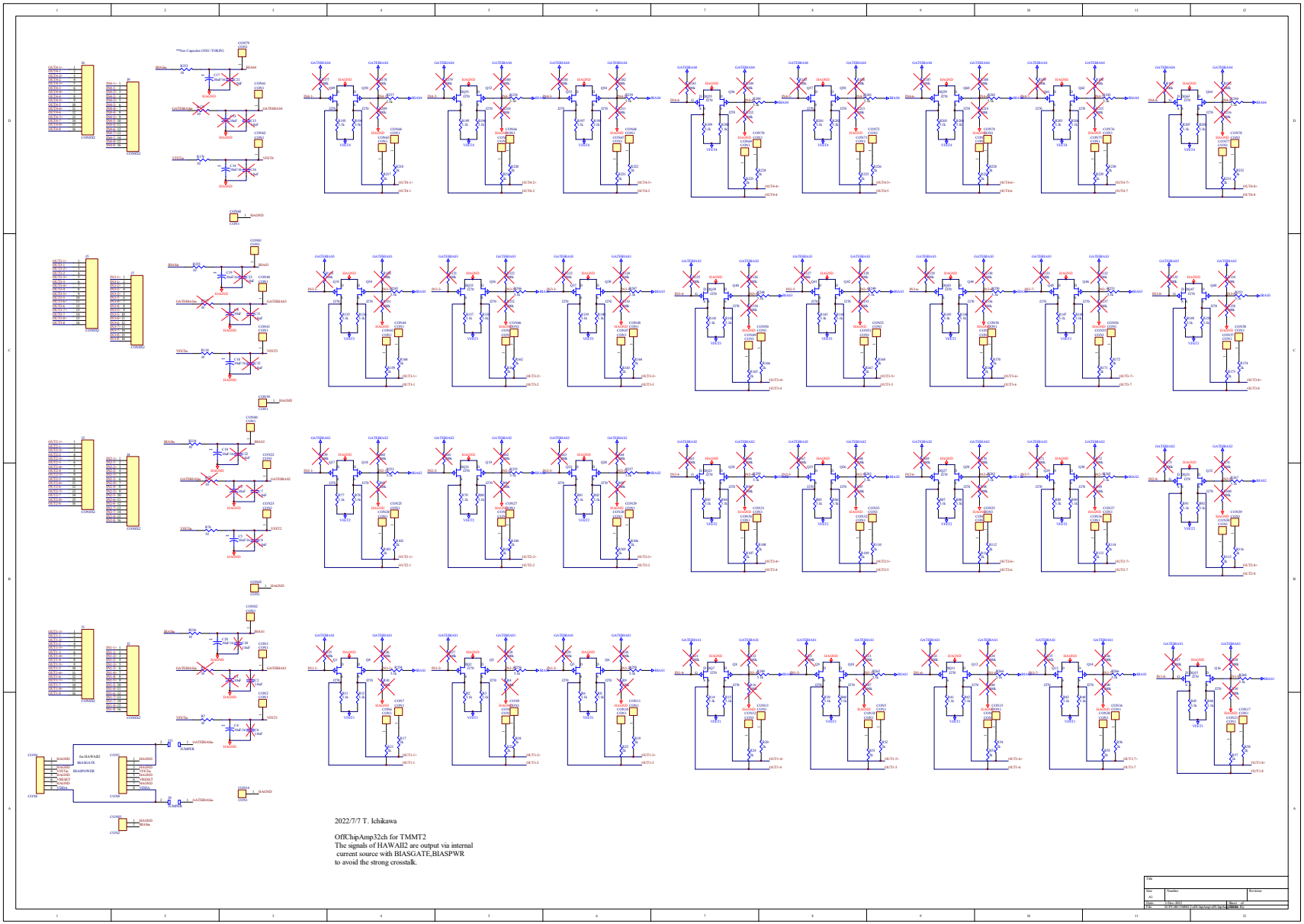
03/24/2003 T.I. V4

06/13/2005 T.I. 10 Mohm deleted from OUTPUT1-8

Title		
Size: A3	Number	Revision
Date: 11-Nov-2005	Sheet of	
File: D:\HAWAII2PCB\HAWAII2\HAWAII32nd.ddb	Drawn By:	



** NeoCapacitor (NEC-TOKIN)
FX2CA2-32
CON24
CON8
CON8X2
VDD
VDDA
BIASGATE
BIASPOWER
VRESET
AGND
HAGND
Title
Size
A2
Number
Revision
Date:
2-Dec-2022
Sheet of
File:
H:\PCB6\TMMT2\HAWAII2\HAWAII32ch.Ddb
Drawn By:



2022/7/7 T. Ichikawa

OffChipAmp32ch for TMMT2
The signals of HAWAII2 are output via internal
current source with BIASGATE,BIASPWR
to avoid the strong crosstalk.

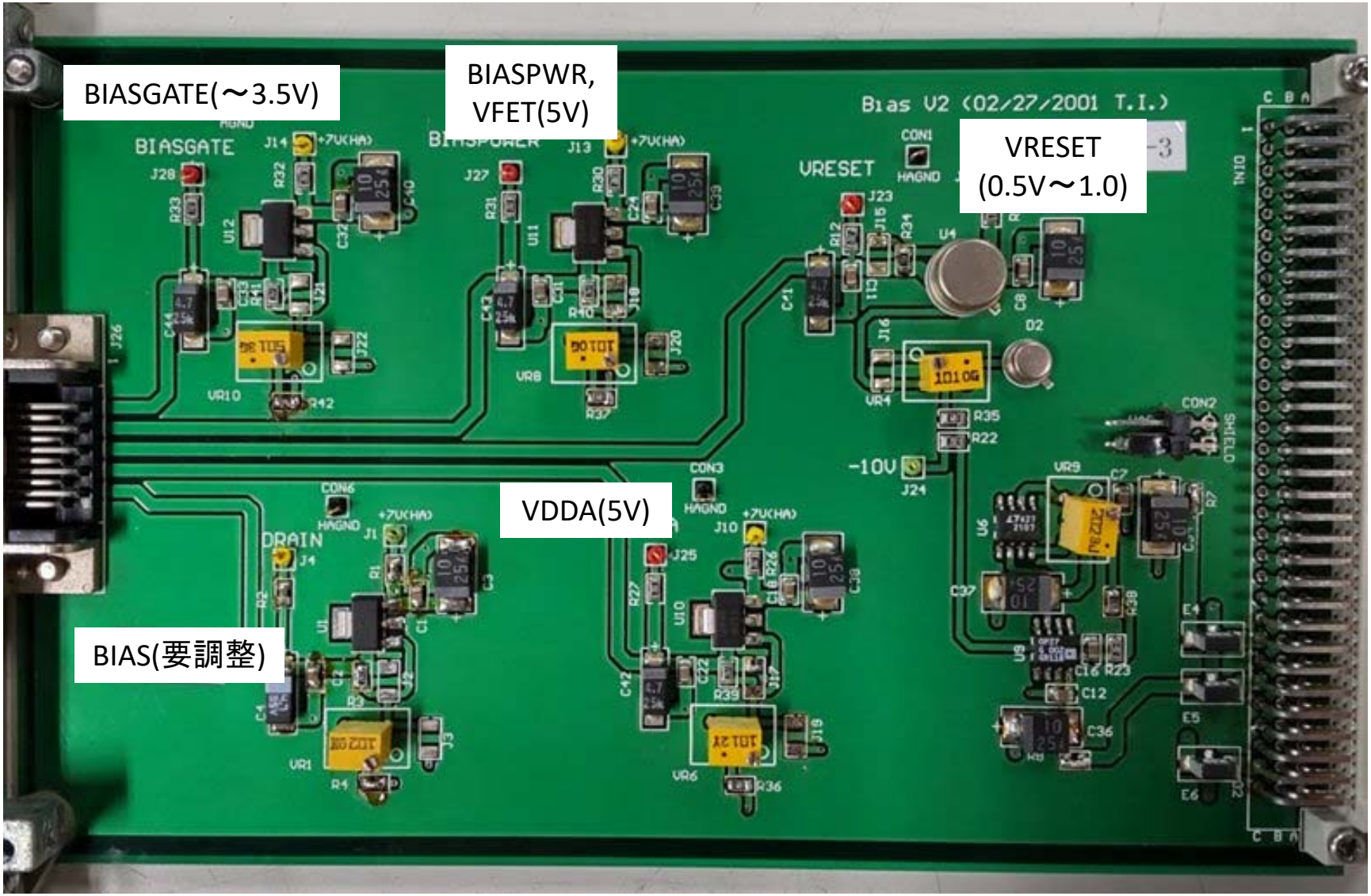
2023/10/4市川

Power & Bias for HAWAII2

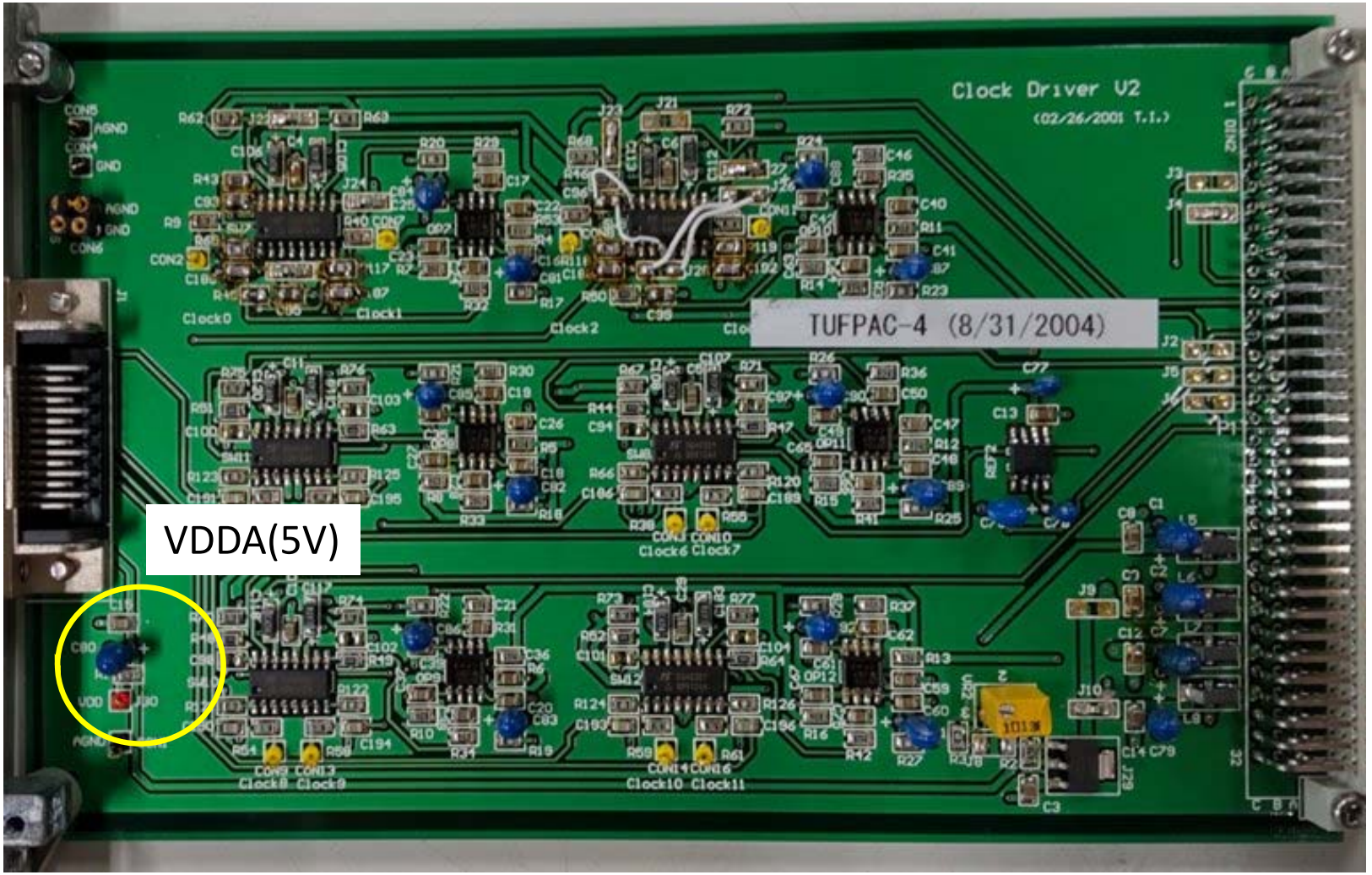
Power Supply	TMMT2 (32ch新読み出し法)	MOIRCS (参考)
VDDA	5V	5V
DRAIN	BIAS of offchipAmp (要調整*)	BIAS=2.3V(offchipAmp)
VDD	5V	5V
BIAS		
BIASPWR	5V, shared with VFET	VFET=5V(offchipAmp)
BIASGATE	BIASGATE (要調整) 3.5Vに設定	GATEBIAS=5V (offchipAmp)
VRESET	0.5V～1V (要調整) 0.5Vに設定	0.5V

電圧の調整

BIAS

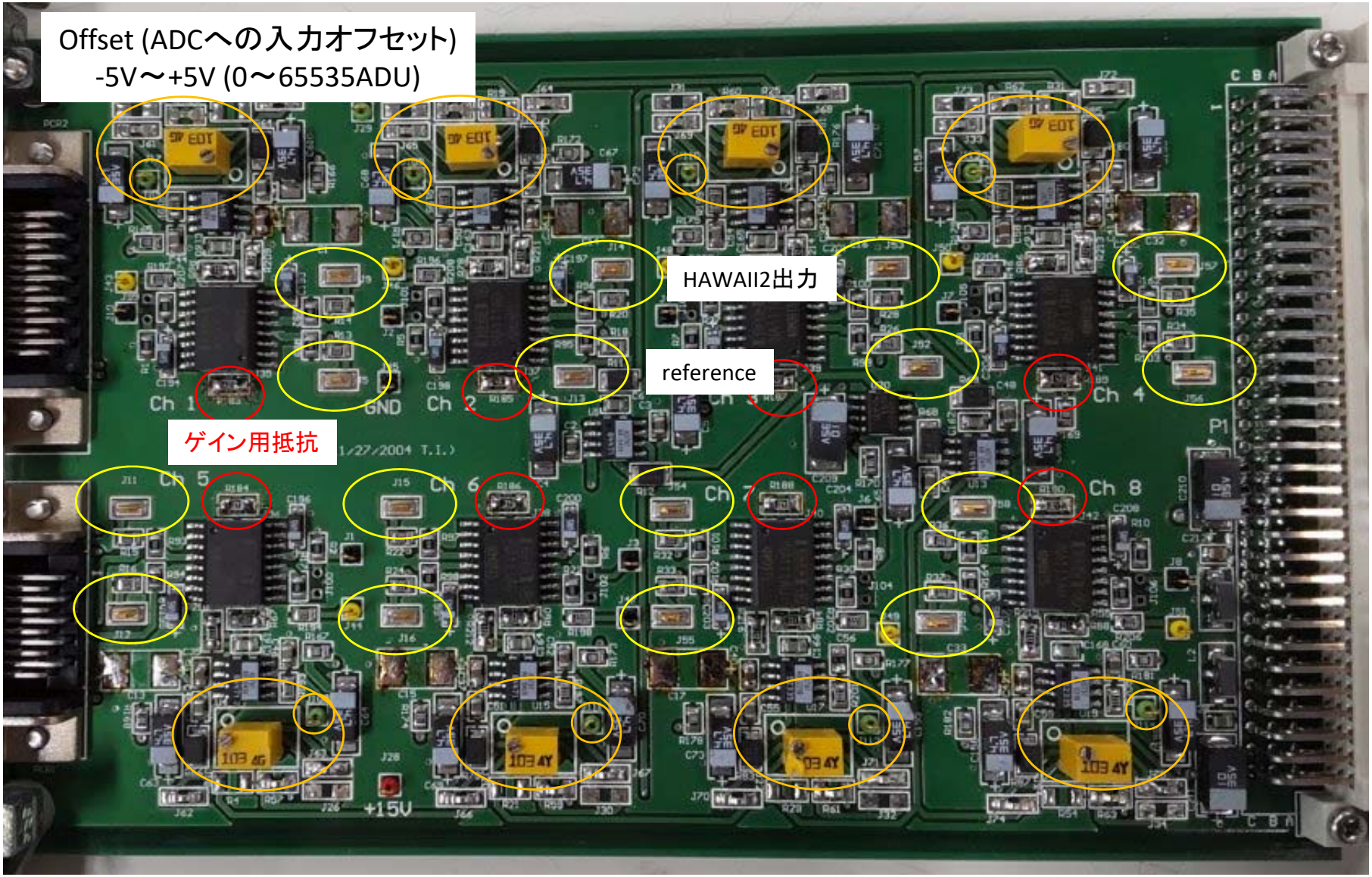

BIASGATE(～3.5V)
BIASPWR,
VFET(5V)
VRESET
(0.5V～1.0)
VDDA(5V)
BIAS(要調整)
Bias V2 (02/27/2001 T.I.)
BIASGATE
VRESET
DRAIN
-10V

Clock Driver



Pre-Amp

INA111アンプのゲインは13.8倍に設定
G=1+50K/R (R=3.9K)
HAWAII2の全出力範囲がADCの入力範囲(±5V)に収まるように選択

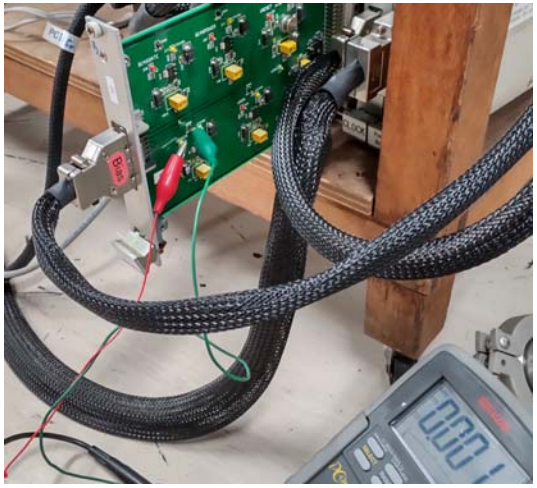


ADCへの入力値=G×(HAWAII2出力－reference)+offset

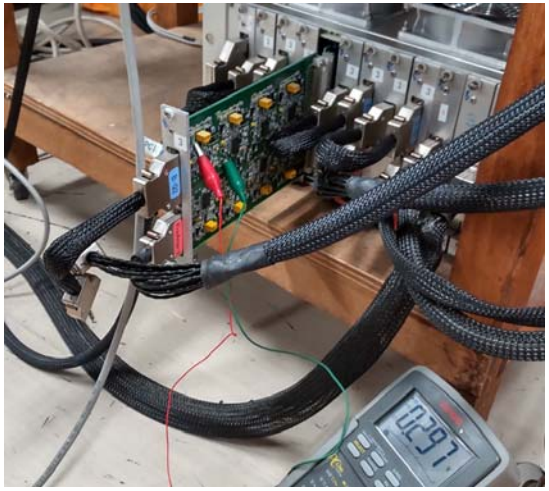
HAWAII2駆動のための電圧調整

冷却下(80K)

1. ダーク-c 0 読み出しでバイアスレベルの調整
   32channel毎の平均値の最低値が～5000ADUになるようにBIASを調整*
2. 光を入れ-c 0読み出しで飽和状態の調整
   32channelすべてで、65535以下(～50000ADU)になるようにPreAmpのオフセット調整*
3. 2.の調整で1.を満足しない場合は、PreAmpのゲインを下げる**



BIASの調整



PreAmpのオフセット調整

*CDS読み出しでキャンセルされる
**それでも調整ができない場合はoffChipAmpのFETの不具合、低温下で異常になることも考えられる

ADCへの入力オフセット*

BIAS	preAmp Gain
2.148V	13.8

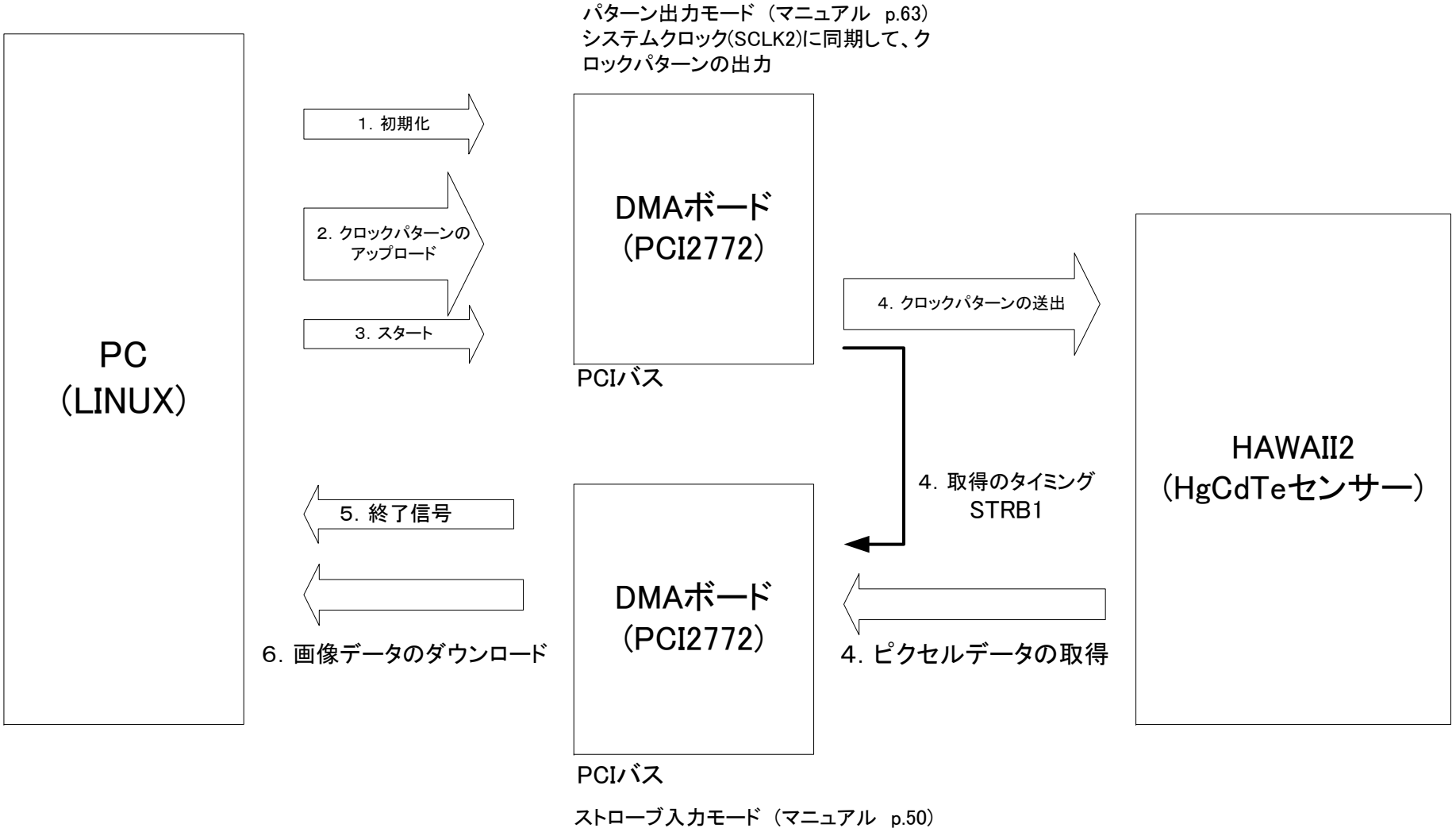
オフセット電圧(2023/10/4)

	O1	O2	O3	O4	O5	O6	O7	O8
Q1	1.014	1.476	0.539	1.222	1.732	0.000	0.725	0.953
Q2	1.334	-0.012	1.232	0.820	2.450	0.000	1.394	1.336
Q3	1.338	0.037	1.326	0.809	0.706	0.175	2.039	1.497
Q4	0.305	1.878	0.426	0.196	1.196	0.162	0.429	0.839

精度は～0.01V

*BIASを変えた時、ボードの交換等がある場合は、再調整が必要
予備ボードも上記の値で予め調整しておく

HAWAII2(TMMT)の読み出し手順(概略)



DMA(direct memory access): PCのCPUを介せずメモリとメモリまたはメモリとI/Oデバイスの間で直接データを転送

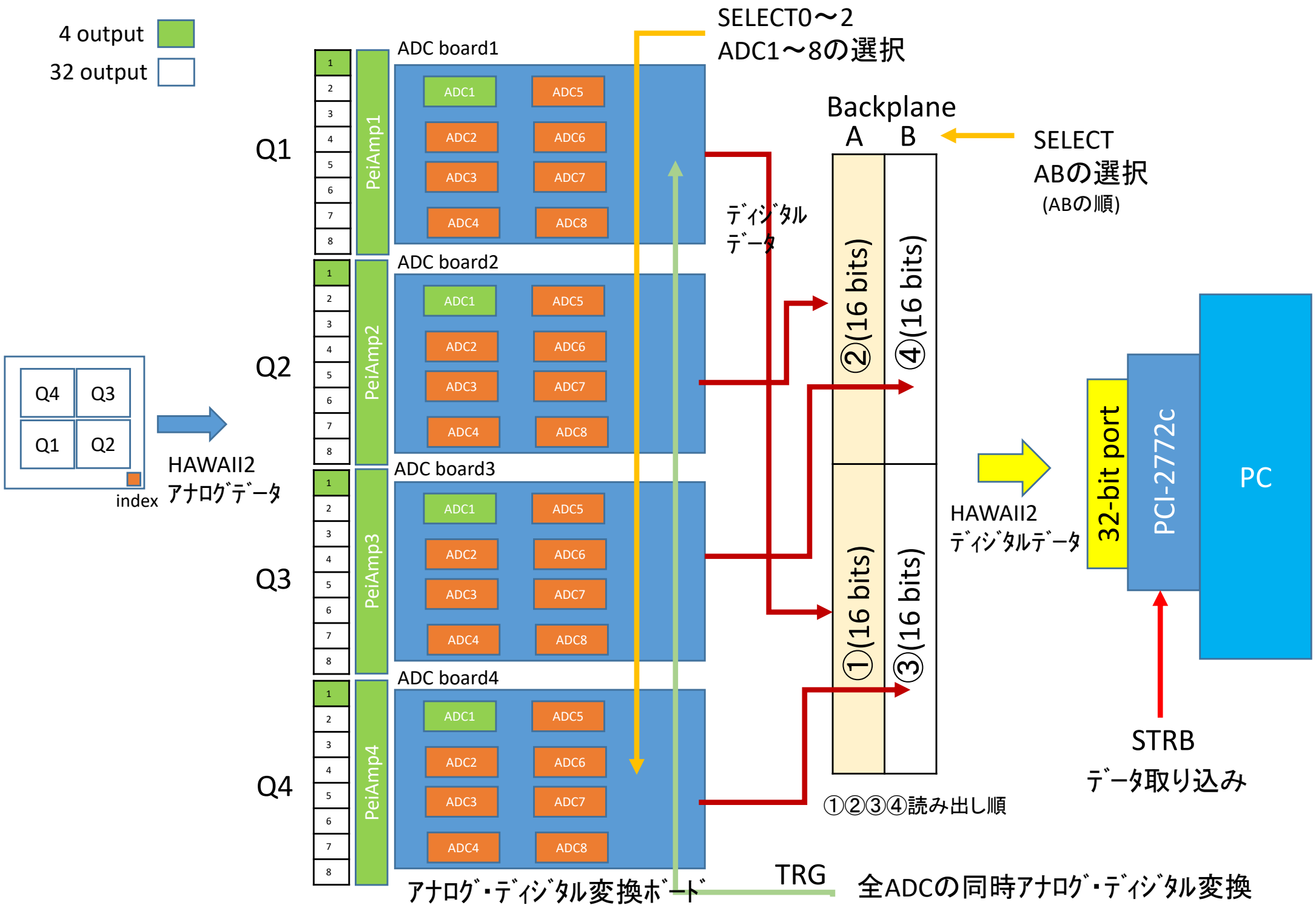
PCI-2772cによる

HAWAII2ディジタルデータの読み出しクロックと手順

2023/9/8
市川隆

Clock*	Name	Data	Target	
0	CLK1	0/1	HAWAII2	
1	SELECT2	0/1	TACS (ADC select)	4ch読み出しの時は000, 32chの場合は 000,001,….,111でADC1～8の出力を選択
2	SELECT1	0/1	TACS (ADC select)	
3	SELECT0	0/1	TACS (ADC select)	
4	FSYNC	0/1	HAWAII2	
5	LSYNC	0/1	HAWAII2	
6	VCLK	0/1	HAWAII2	
7	RESET	0/1	HAWAII2	
8	READ	0/1	HAWAII2	
9	RESETEN	0/1	HAWAII2	
10	O1	0/1	HAWAII2	
11	(NOT USED)			
12	(NOT USED)			
13	BUS SELECT	0/1	TACS (bus select)	A(1),B(0)バスの選択
14	STRB1	1→0	PCI-2772c	PCI-2772cでのデータ取り込み(MOIRCSでは不要)
15	ADC TRIG	1→0	TACS	ADC変換

*CLK2, CLKB1, CLKB: CLK1を用いてｸﾛｯｸﾎﾞｰﾄﾞで生成
O2=0、LRST=1: configﾎﾞｰﾄﾞ内で固定


4 output
32 output
SELECT0～2
ADC1～8の選択
Backplane
A B
SELECT
ABの選択
(ABの順)
ADC board1
ADC board2
ADC board3
ADC board4
ADC1
ADC2
ADC3
ADC4
ADC5
ADC6
ADC7
ADC8
PeiAmp1
PeiAmp2
PeiAmp3
PeiAmp4
Q1
Q2
Q3
Q4
Q4 Q3
Q1 Q2
index
HAWAII2
ｱﾅﾛｸﾞﾃﾞｰﾀ
ﾃﾞｨｼﾞﾀﾙ
ﾃﾞｰﾀ
②(16 bits)
④(16 bits)
①(16 bits)
③(16 bits)
①②③④読み出し順
HAWAII2
ﾃﾞｨｼﾞﾀﾙﾃﾞｰﾀ
32-bit port
PCI-2772c
PC
STRB
ﾃﾞｰﾀ取り込み
TRG
全ADCの同時ｱﾅﾛｸﾞ･ﾃﾞｨｼﾞﾀﾙ変換
ｱﾅﾛｸﾞ･ﾃﾞｨｼﾞﾀﾙ変換ﾎﾞｰﾄﾞ

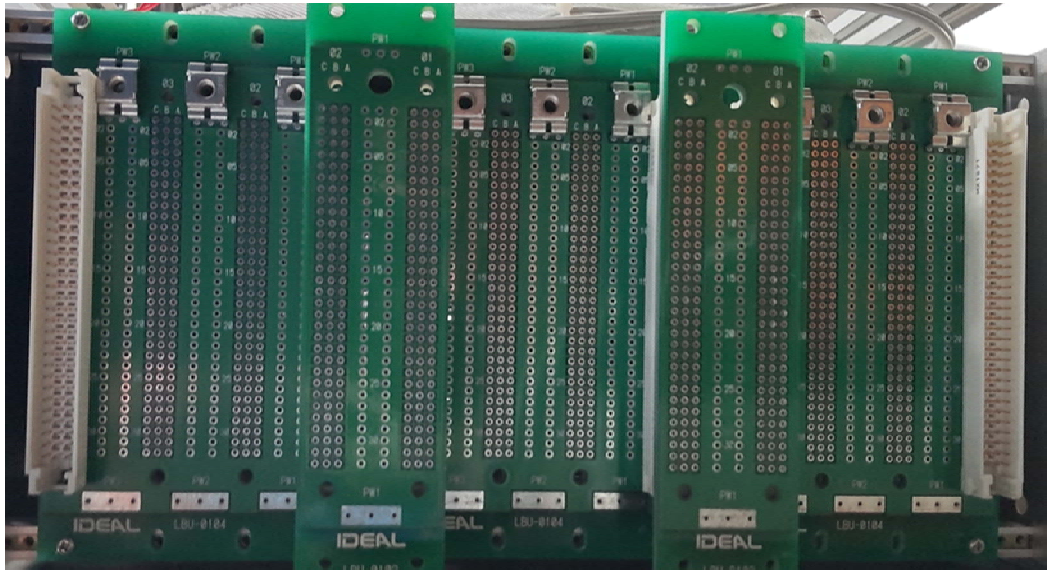
TACS

制御パソコン

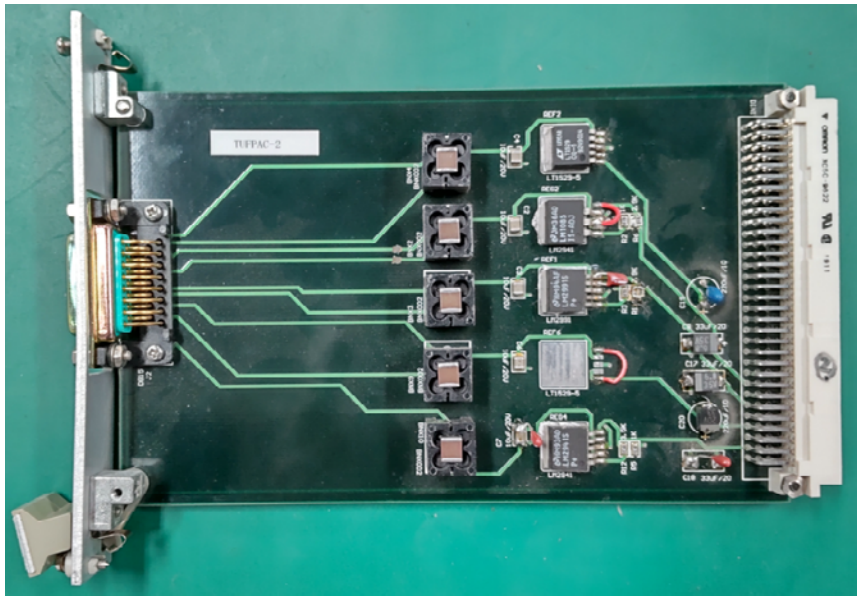
パネル

電源

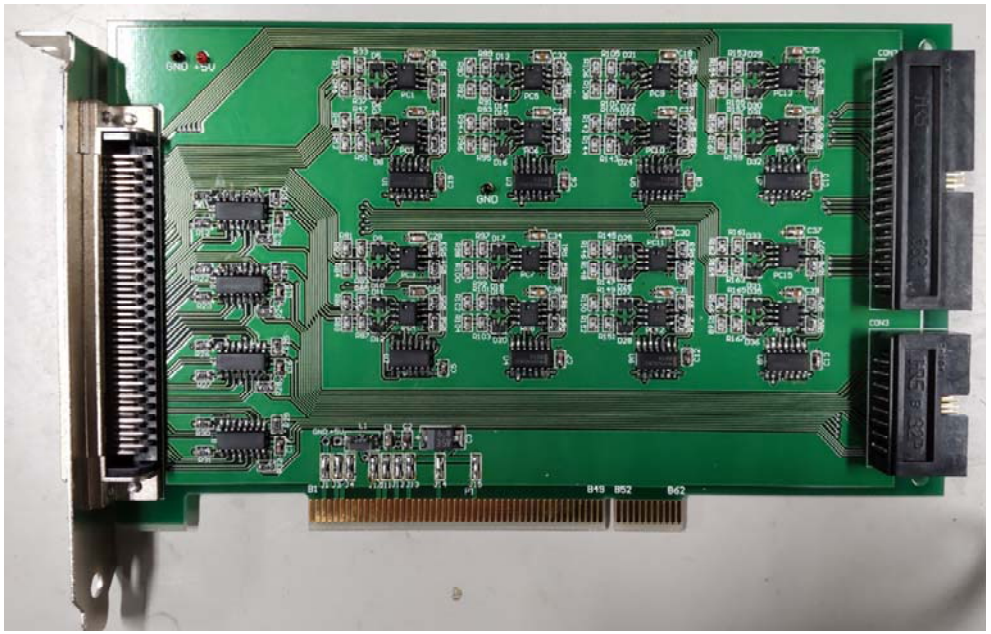
3Uユニバーサルバックプレーン



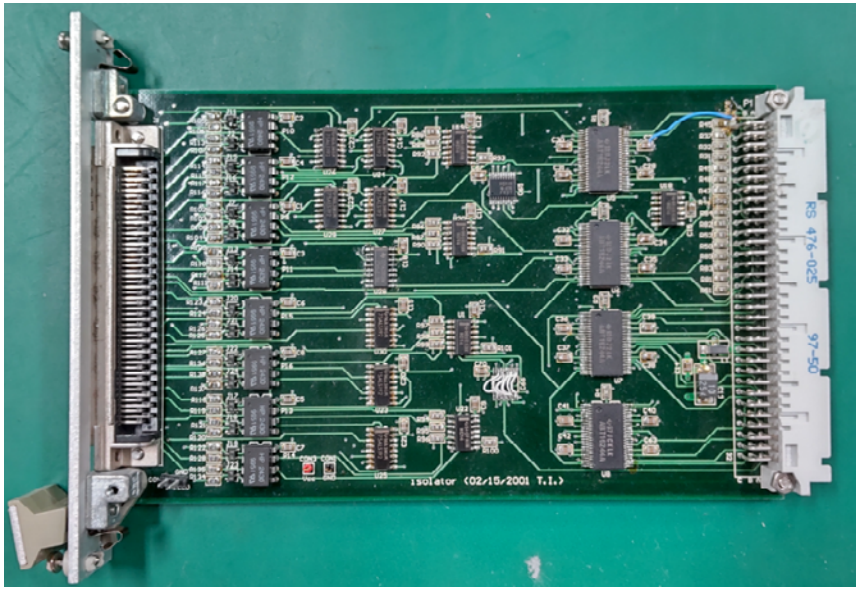
PowerRCV



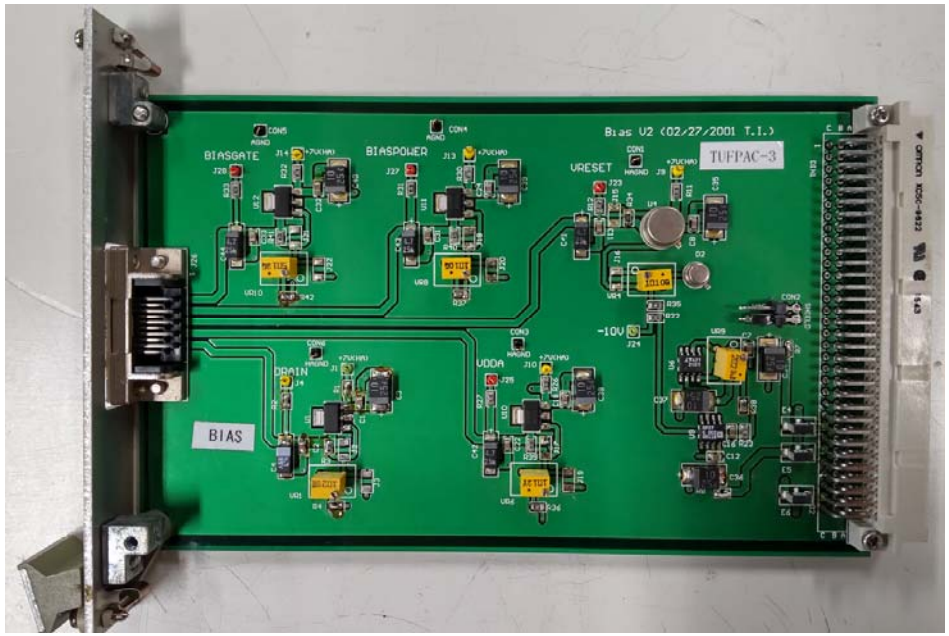
Isolation PIO



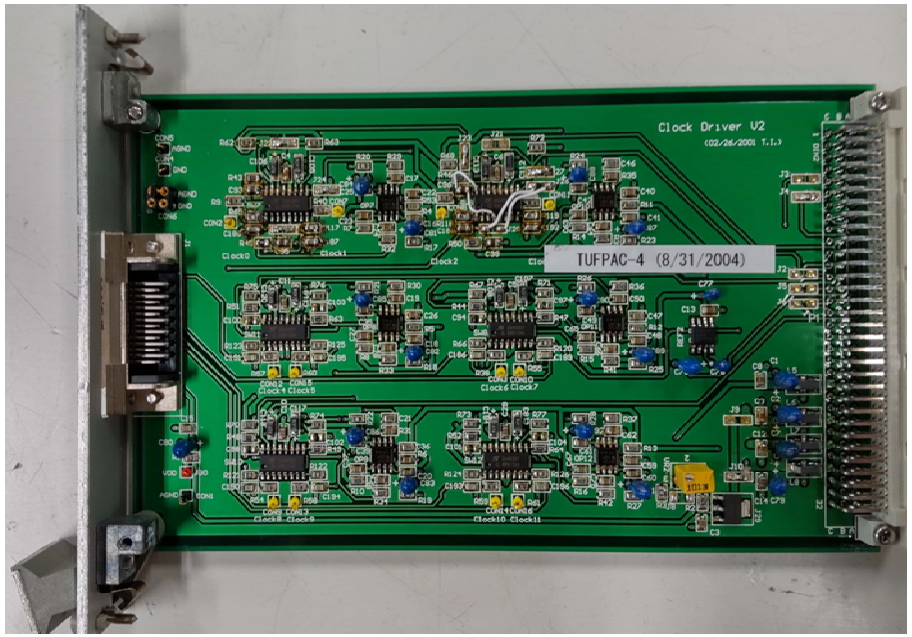
Isolator



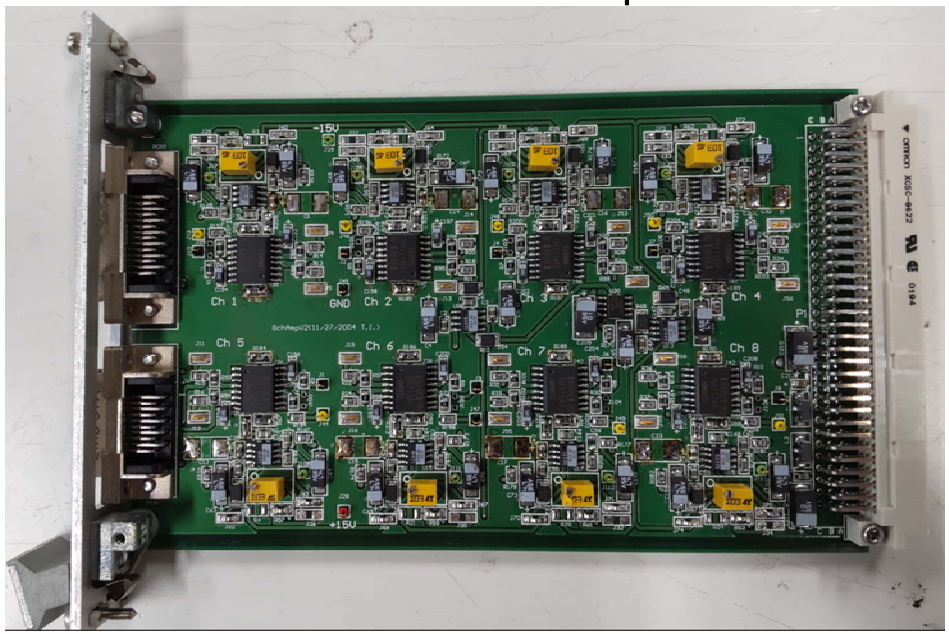
Bias



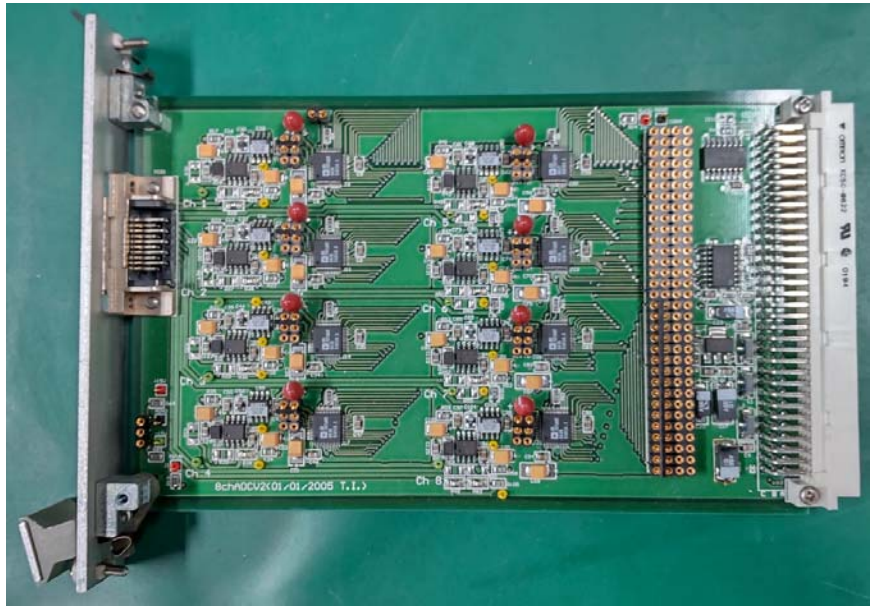
Clock Driver



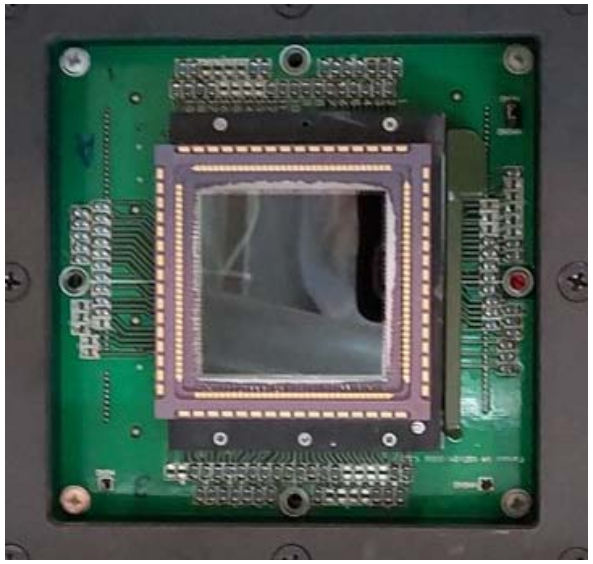
8ch Pre Amp



8ch ADC



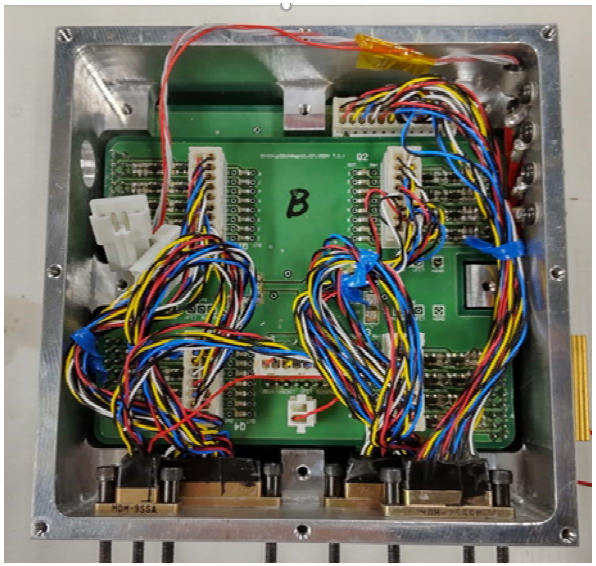
HAWAII2 2048x2048 HgCdTe



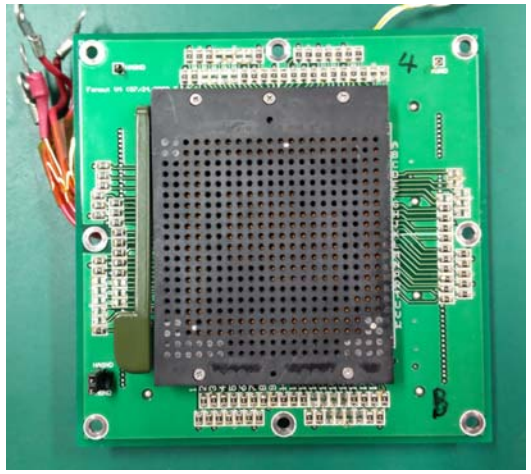
Array box

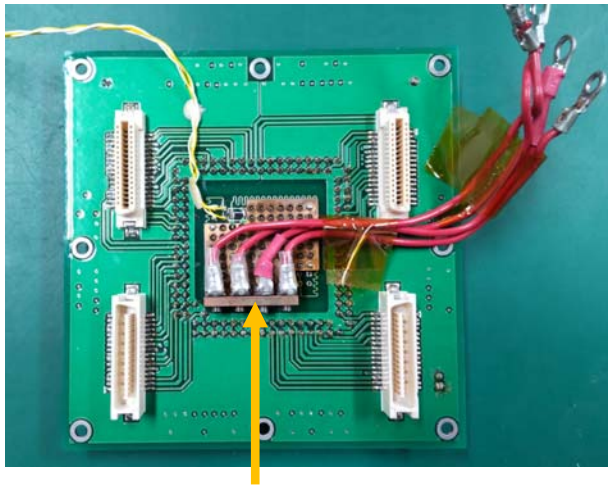
ZIFソケット

Array box (底面配線)



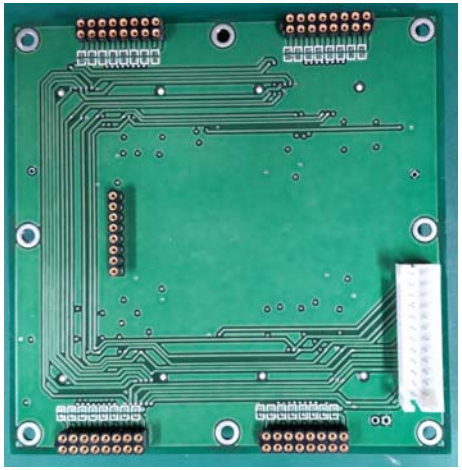
Fanout





ヒートシンク

Config



OffchipAmp